128Kx32 SRAM MULTICHIP PACKAGE RADIATION TOLLERANT

WS128K32-XG2TXE

***ADAVANCED**

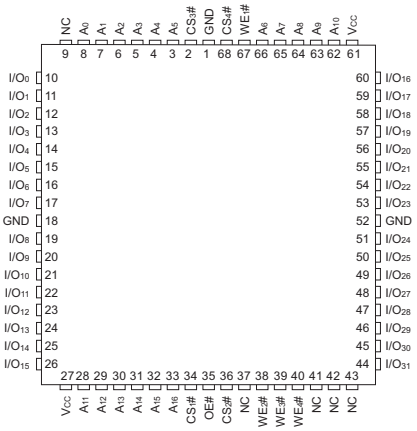
FEATURES

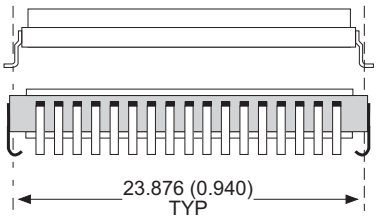
- Access Times of 35, 45, 55ns
- Packaging
  - 68 lead, 22.4mm CQFP (G2T), 4.57mm (0.180"), (Package 509)
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Low Power Data Retention
- Commercial, Industrial and Military Temperature Ranges
- 5V Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  - WS128K32-XG2TXE – 8 grams typical
- Radiation tolerant with epitaxial layer on die.
- 6T memory cells provide excellent protection against soft errors

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

FIGURE 1 – PIN CONFIGURATION FOR WS128K32N-XG2TXE

TOP VIEW



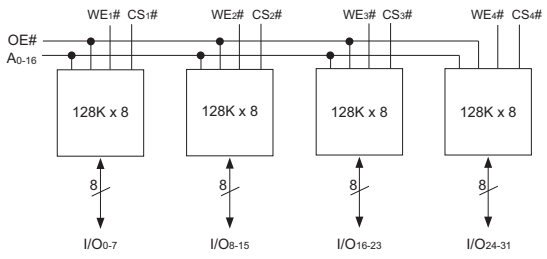


The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O_{0-31}	Data Inputs/Outputs
A_{0-16}	Address Inputs
WE_{1-4}#	Write Enables
CS_{1-4}#	Chip Selects
OE#	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	V_{CC}+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Opertating Temp. (MIL)	T_A	-55	+125	°C

RADIATION CHARACTERISTICS

Total Dose (TM1019.5)			**Latch-up** 25°C V_{CC} Max	**SEU LET Threshold** (V_{CC} MIN)	**Cross Section** /BIT
Functional	**Parametric**				
(Krads)	(Krads)	Typical Iccsb (mA)	**(MeV/mg/cm2)**	**(MeV/mg/cm2)**	**(E-6 cm2)**
30	30	1.2	>100	2	0.2

TRUTH TABLE

CS#	OE#	WE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C_{OE}	V_{IN} = 0V, f = 1.0 MHz	50	pF
WE_{1-4}# capacitance CQFP G2T	C_{WE}	V_{IN} = 0V, f = 1.0 MHz	20	pF
CS_{1-4}# capacitance	C_{CS}	V_{IN} = 0V, f = 1.0 MHz	20	pF
Data# I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	CS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		520	mA
Standby Current	I_{SB}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		8	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -40mA, V_{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

-55°C ≤ T_A ≤ +125°C

Characteristic	Sym	Conditions	Min	Max	Units
Data Retention Voltage	V_{CC}	V_{CC} = 2.0V	2	—	V
Data Retention Quiescent Current	I_{CCDR}	CS ≥ V_{CC} -0.2V	—	1	mA
Chip Disable to Data Retention Time (1)	T_{CDR}	V_{IN} ≥ V_{CC} -0.2V	0	—	ns
Operation Recovery Time (1)	T_R	or V_{IN} ≤ 0.2V	T_{RC}	—	ns

NOTE: Parameter guaranteed, but not tested.

AC CHARACTERISTICS

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Read Cycle	Symbol	-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		55		ns
Address Access Time	t_{AA}		35		45		55	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip Select Access Time	t_{ACS}		35		45		55	ns
Output Enable to Output Valid	t_{OE}		15		20		30	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	3		3		3		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		20		20		20	ns
Output Disable to Output in High Z	t_{OHZ}[1]		12		15		20	ns

1. This parameter is guaranteed by design but not tested.

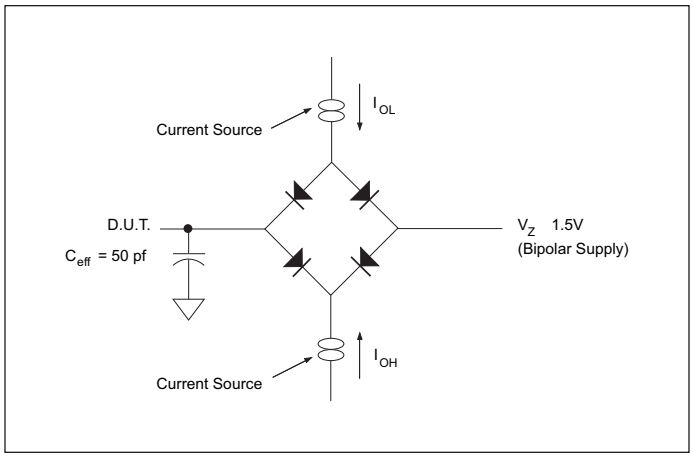
AC CHARACTERISTICS

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Write Cycle	Symbol	-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	35		45		55		ns
Chip Select to End of Write	t_{CW}	25		35		45		ns
Address Valid to End of Write	t_{AW}	25		35		45		ns
Data Valid to End of Write	t_{DW}	20		25		25		ns
Write Pulse Width	t_{WP}	25		35		45		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Output Active from End of Write	t_{OW}[1]	0		0		0		ns
Write Enable to Output in High Z	t_{WHZ}[1]		10		15		20	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIGURE 2 – AC TEST CIRCUIT

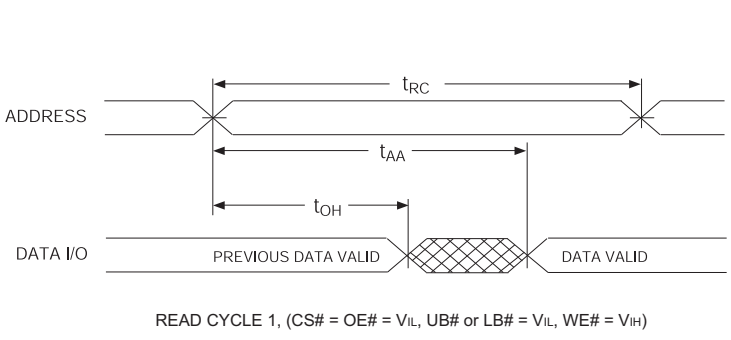


AC TEST CONDITIONS

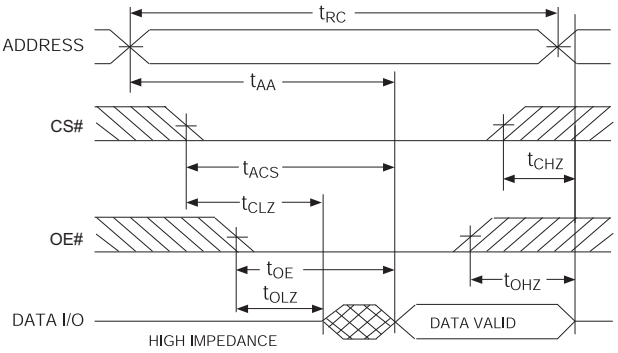
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIGURE 3 – TIMING WAVEFORM – READ CYCLE

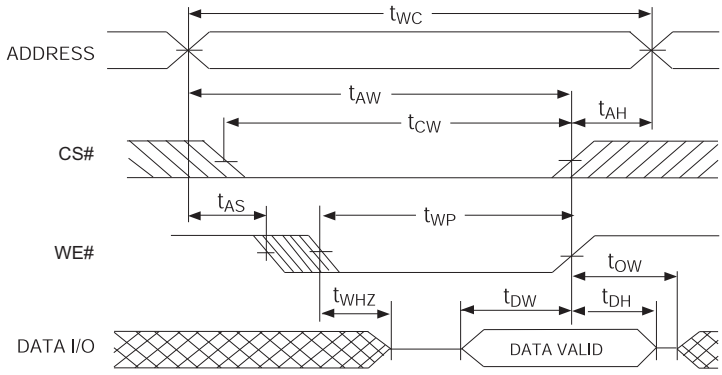


READ CYCLE 1, (CS# = OE# = V_{IL}, UB# or LB# = V_{IL}, WE# = V_{IH})



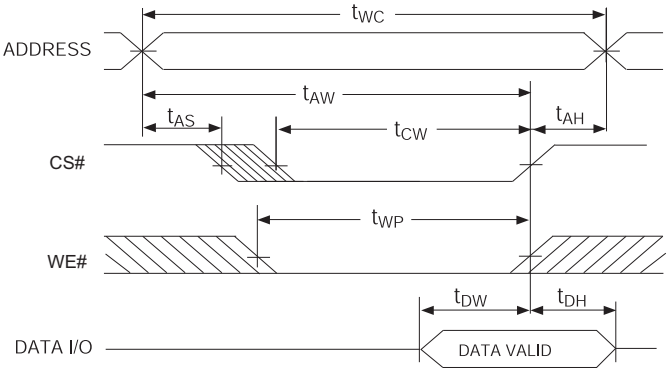
READ CYCLE 2 (WE# = V_{IH})

FIGURE 4 – WRITE CYCLE – WE# CONTROLLED



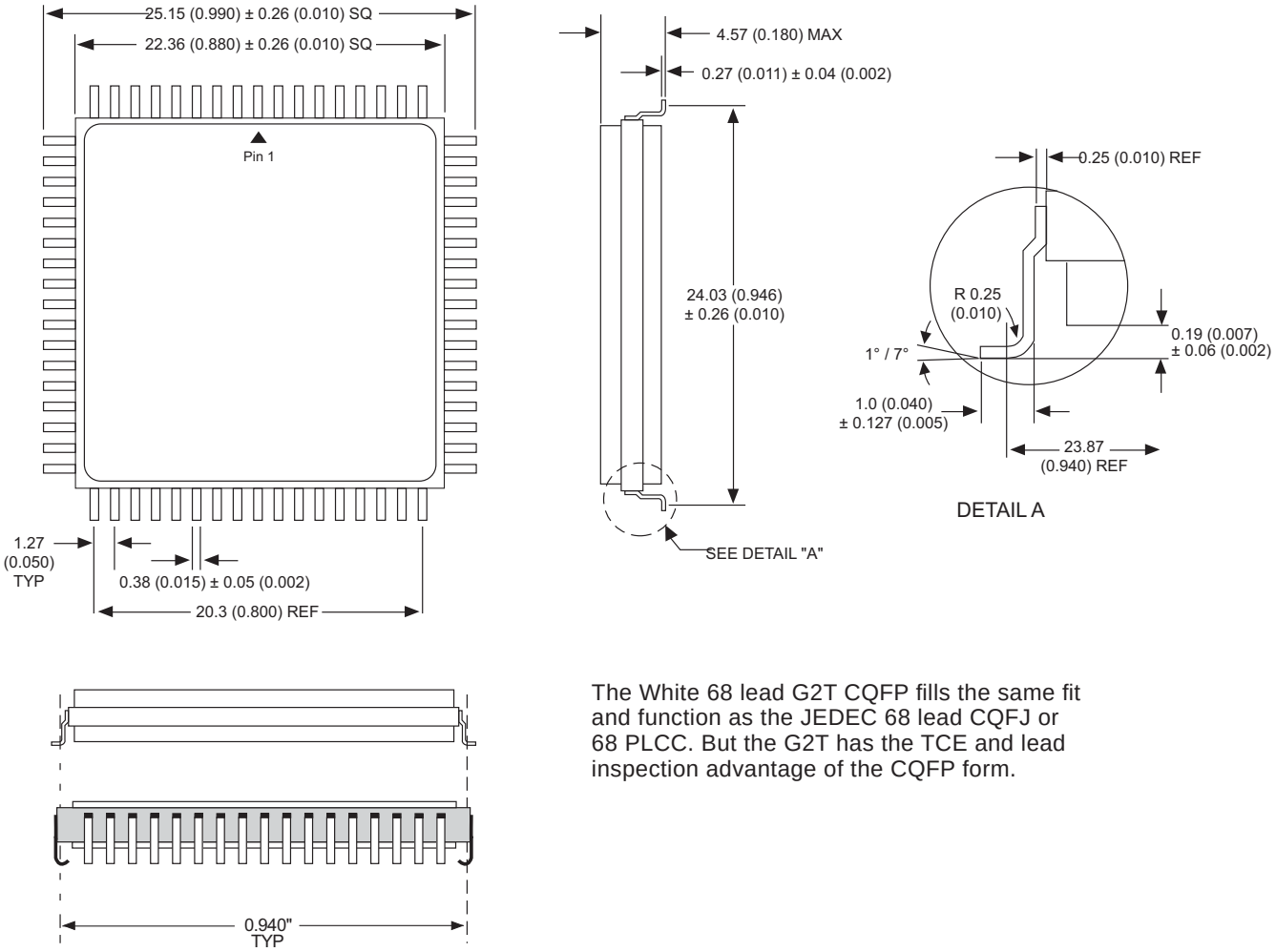
WRITE CYCLE 1, WE# CONTROLLED

FIGURE 5 – WRITE CYCLE – CS# CONTROLLED



WRITE CYCLE 2, CS# CONTROLLED

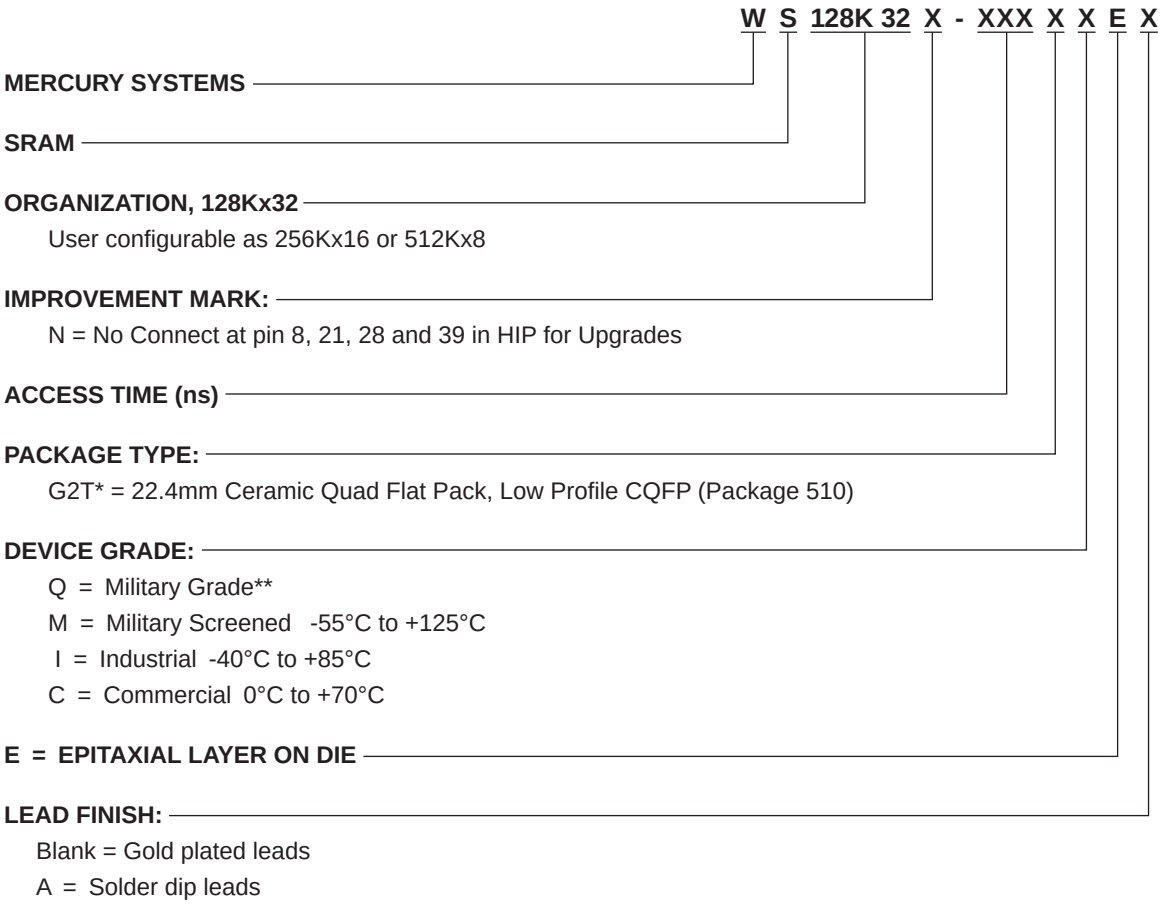
PACKAGE 510 – 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)



The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



* Low Power Data Retention only available in G2T Package Type
** This product is processed the same as the 5962-XXXXXHXX product but all test and mechanical requirements are per the Mercury Systems data sheet.

Document Title

128Kx32 SRAM MULTICHIP PACKAGE, RADIATION TOLLERANT

Revision History

Rev #	History	Release Date	Status
Rev 1	Changes (Pg. 1-7) 1.1 Change document layout from White Electronic Designs to Microsemi 1.2 Add document Revision History page	May 2011	Advanced
Rev 2	Change (Pg. 6) 2.1 Changed Device Grade "Q" description from "MIL-STD-883 Compliant" to "MIL-PRF-38534 Class H Compliant."	May 2014	Advanced
Rev 3	Change (Pg. 6) 3.1 Changed Device Grade "Q" description from "MIL-PRF-38534 Class H Compliant." to "Military Grade."	August 2014	Advanced
Rev 4	Changes (Pg. All) (ECN 10156) 4.1 Change document layout from Microsemi to Mercury Systems	August 2016	Advanced