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Model 5560
3U VPX SOSA aligned Versal® ACAP board delivers massive data throughput

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The Model 5560 is a coprocessing 3U VPX SOSA aligned FPGA board powered by Versal® HBM (high-bandwidth memory) technology. This board is ideal for highly compute-intensive applications that must stage or buffer massive amounts of data in memory but must also have extremely high-bandwidth access to that data. Combining HBM technology processing logic with four 100 GigE interfaces, delivering an aggregate data throughput rate of 50 GB/sec, supports enormous data ingest from new higher-speed converters. A Navigator® FPGA design kit (FDK) and board support package (BSP) provide operational control of the hardware and easy configuration of new FPGA functions.

FAQ

What is SOSA and why is it important?
The SOSA open standard has been created to improve subsystem reconfigurability, upgradability and reuse, and to shorten cycle times for countering emerging threats in SIGINT, radar, EW and communications applications. By employing SOSA specified products, users can expect to find a reliable and very well-defined standard architecture for development and deployment.

What VPX profile DOES the 5560 board conform to?
Per the SOSA specification, the 5560 follows the SLT3-PAY-1F1U1S1S1U2F1H-14.6.11-12 profile.

What ACAP is used on the 5560?
The board features a Xilinx/AMD Versal HBM VH1542.

What advantages does the Versal ACAP offer?
The heterogeneous mix of Versal ACAP resources gives designers the freedom to assign compute power to the processing engine most suitable to the task at hand, and the ability to adaptively reassign resources as required. Different members of the ACAP family provide various blends of three major processing resources: scalar processors (ARM CPUs), adaptable logic (FPGAs), and vector processors (GPUs and DSPs). This flexibility of ACAP delivers as much as ten times the performance over dedicated processor types alone.

What is HBM and why is it important?
High-bandwidth memory, or HBM, is 16 GBs of on-chip SDRAM. Having the SDRAM directly on the ACAP allows much higher-speed access to the memory. It supports memory bandwidths of up to 820 GB/sec and represents an 8x throughput increase over traditional external DDR5 SDRAM, which is critical for high data bandwidth and high-computational applications.

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In addition to the HBM, is there any other memory on the board?

Yes. An external 8 GB DDR4 SDRAM bank is available to the ACAP and is typically used by the ACAP's Scalar Engines for processing and operating system support

In addition to the HBM, what other resources are available on the VH1542?

System Logic Cells – 3.8 million, DSP slices – 7,392, UltraRAM –366 Mb

Does the board support optical interfaces and at what speeds?

Yes. The board supports four 8-lane optical interfaces, running at 25 Gbps per lane, that appear on the VITA 67.3C connector. Users can install their own protocol or use the 100 GigE UDP IP core supplied with the Navigator FPGA Design Kit to instantiate the 100 GigE interfaces.

How quickly can I get up and running with the 5560?

The board is shipped with factory-installed IP that loads the ACAP from onboard FLASH on power up. The IP-based functions are specific and appropriate to match the hardware features of the board, including support for the 10, 40 and 100 GigE interfaces. Software libraries to support the built-in functions and pre-compiled examples allow the board to be used right out of the box.

Can the built-in IP be changed?

Yes. While the built-in IP satisfies the need to confirm operation and move data on and off the board, users look to the high-performance processing available in the ACAP for custom processing. The Mercury Navigator FPGA Design Kit works with Xilinx Vivado and includes all installed IP cores as well as a library of additional functions for users to add to, modify or completely replace the factory installed IP. The Mercury Navigator Board Support Package is the companion product of the FDK providing software support for all IP and hardware functions.

What factory-installed IP is included with the 5560?

Because the processing tasks performed on the 5560 will be different for every application, the built-in IP is more generic, providing support for the board's 10 GigE, 40 GigE and PCIe interfaces. In addition, the Navigator FPGA Design Kit IP core library contains many functions, like the 100 GigE UDP Ethernet interface, which can be installed by the user as needed.

What applications can the 5560 be used for?

The 5560 can be deployed in a wide range of applications including systems that require high-performance processing and memory and I/O bandwidth.

The 5560 is an ideal coprocessor when paired with the Mercury 5550 or 5553 RFSoC-based boards. The 5560's 100 GigE data paths provide a high-speed interface for exchanging data with the RFSoC boards.

The 5560 is also an excellent match for high data processing applications like data analytics, adaptable artificial intelligence, image processing and target identification.

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