AM9024 – Transceiver Module

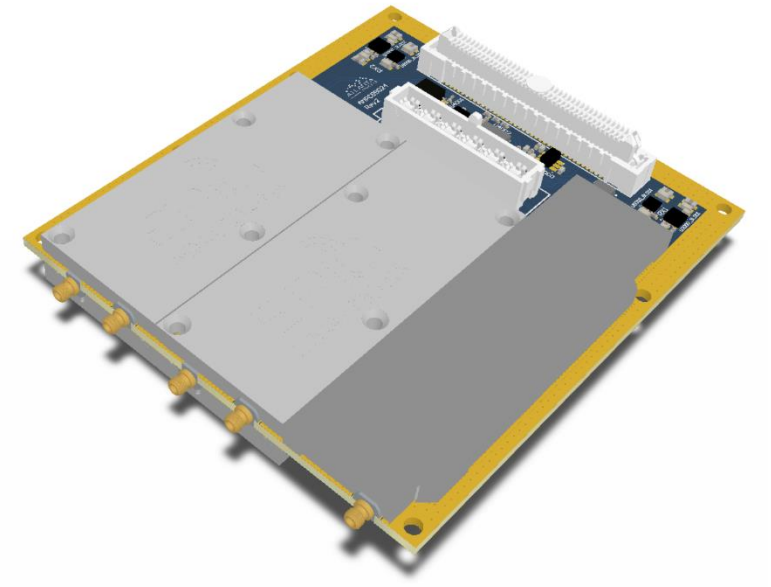
4 Receive, 1 Transmit 0.01 GHz to 18 GHz

AM9024 is a fully integrated FMC sized module with four receive channels and one transmit channel covering 6 GHz to 18 GHz with 1000 MHz instantaneous bandwidth. AM9024 also offers direct feed through of signals from 10 MHz to 6 GHz in both the transmit and receive channels. The super-heterodyne tuner module is designed for high performance and low size, weight, and power (low SWaP) and is easily mounted to a host circuit board for signal processing and control. In each channel sub-octave pre-selectors, pre-amplifiers, local oscillators, frequency converters, power and control line filtering, low drop-out regulators, and channel control FPGAs are included and for the full module two temperature sensors are provided for temperature gradient across the board.

The analog IF output frequency of the receive channels and analog IF input frequency of the transmit channel are centered at 3 GHz with a 1000 MHz instantaneous bandwidth. The four receive channels can be configured for phase coherent operation allowing for applications such as beam forming and direction finding. Interfacing to the individual channels is accomplished by providing RF input, DC voltages, a 100 MHz differential frequency reference, and SPI control.

FEATURES

- 6 GHz to 18 GHz Receive Channel Down-Convert
- 6 GHz to 18 GHz Transmit Channel Up-Convert
- Sub 6 GHz Direct Feed Through for Transmit and Receive Channels
- 1000 MHz Bandwidth
- 3 GHz IF Output Frequency
- Sub-Octave Preselection
- Channel Low Power and Sleep Modes
- Channel Disable
- Two Temperature Sensors
- RX: 5 dB ± 3dB Gain
- RX: <10 dB Noise Figure, >+4 dBm IIP3
- TX: 5 dB ± 3dB Gain, 0 dBm output
- TX: +24 dBm OIP3
- +3.6V and +5.5V DC Input
- 16.2 W Typical Power Consumption
- -20C to +70C Operation
- 3.10" x 2.72" x 0.34" (78.80 x 69.00 x 8.69 mm)



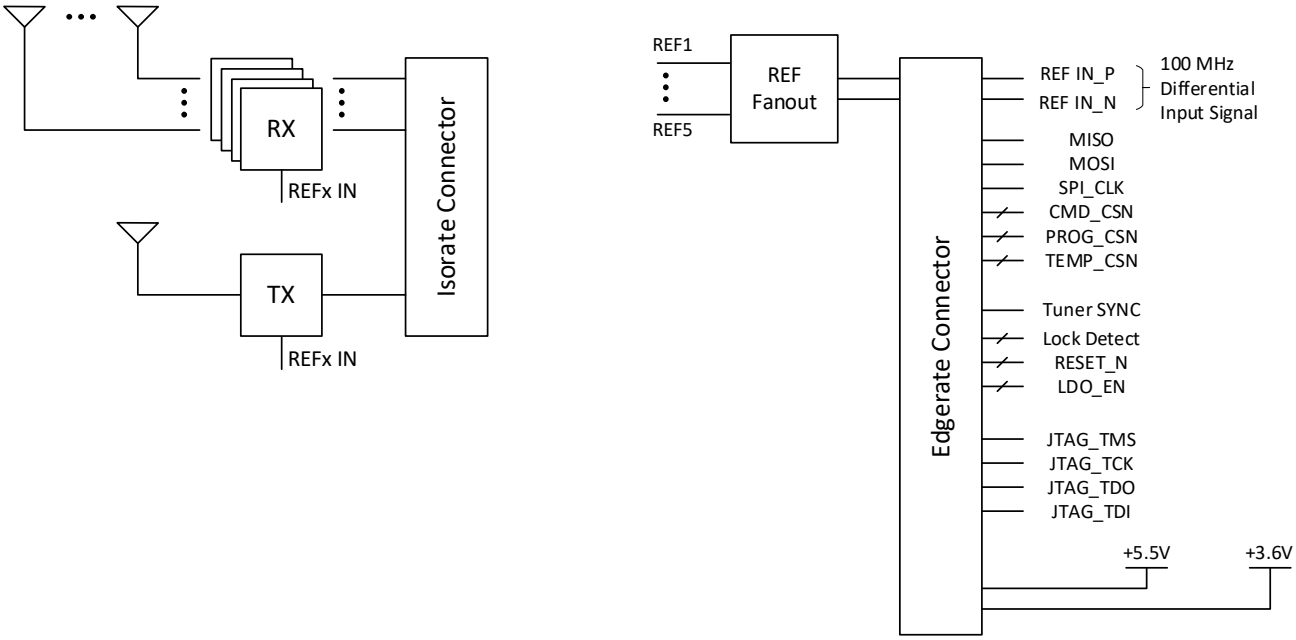
CONTENTS

REVISION HISTORY

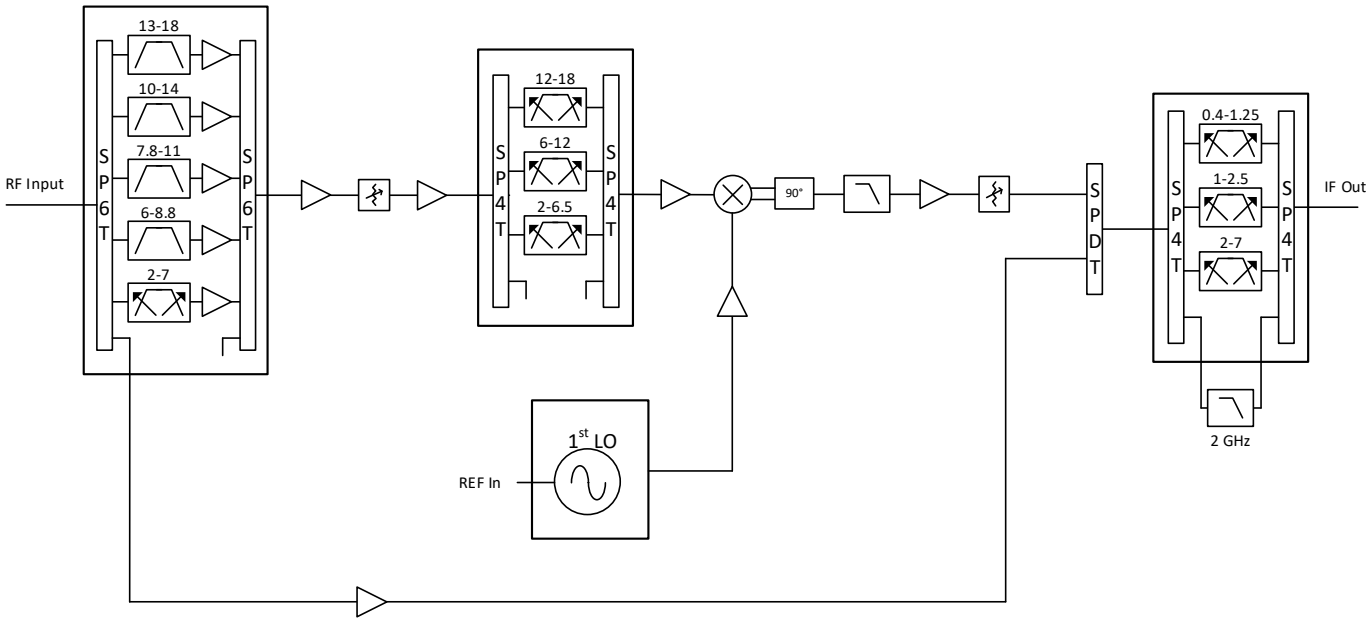
Date	Revision	Notes
February 26, 2021	0	Preliminary Release.
April 23, 2021	1	Initial Release.
July 25, 2022	2	Updates for AM9024 Rev3.
October 13, 2023	3	Updated for ITAR disclaimer, Mercury Logo added. Plots and RF Performance updated for Rev4 PCB changes.
September 10, 2024	4	Changed to Mercury branding. No content changes.
April 1, 2025	5	Public release, latest spec performance

BLOCK DIAGRAM

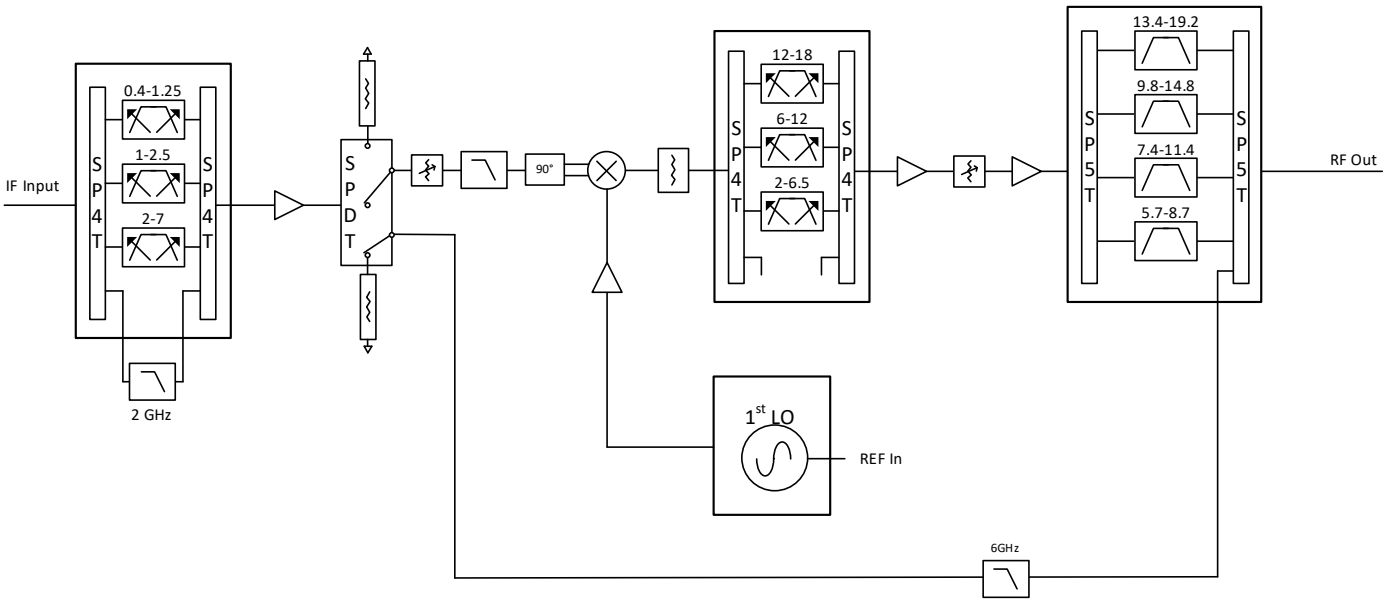
Top Level



Receive Channel



Transmit Channel



SPECIFICATIONS

Absolute Maximum Ratings

	Testing Condition	Minimum	Maximum
RF Input Power	Receive Channel		+20 dBm
IF Input Power	Transmit Channel	-5 dBm	+10 dBm
+5.5 VDC Supply			+6.5 V
+3.6 VDC Supply			+7.0 V
LDO_ENx			+6.5 V
Operating Temperature		-40 C	+85 C
Storage Temperature Range		-55 C	+150 C

Note: Any device operation beyond the Absolute Maximum Ratings may result in permanent damage to the device. The values listed in this table are extremes and do not imply functional operation of the device at these or any other conditions beyond what is listed under Recommended Operating Conditions. Any part subjected to conditions outside of what is recommended for an extended amount of time may suffer from reliability concerns.

Handling Information

	Minimum	Maximum
Storage Temperature Range (Recommended)	-50 C	+125 C

Mercury products are electrostatic sensitive.
Follow safe handling practices to avoid damage.

Recommended Operating Conditions

	Minimum	Typical	Maximum
+5.5 VDC Supply	+5.4 V	+5.5 V	+6.0 V
+3.6 VDC Supply	+3.5 V	+3.6 V	+4.0 V
Operating Case Temperature	-20 C		+70 C

DC ELECTRICAL CHARACTERISTICS

(T = 25 °C unless otherwise specified)

Parameter	Notes	Min	Typical	Max
Logic Level Low		0 V		+0.8 V
Logic Level High		+2.0 V		+3.5 V

Parameter	Notes	+3.6V Typical	+5.5V Typical
Current Dissipated	Single RX Down Convert EN	740 mA	105 mA
	Single RX Feed Through	480 mA	130 mA
	Single RX Low Power Mode*	480 mA	15 mA
	Single RX Sleep Mode**	40 mA	15 mA
	TX Up Convert EN	620 mA	135 mA
	TX Feed Through	360 mA	135 mA
	TX Low Power Mode*	360 mA	20 mA
	TX Sleep Mode**	40 mA	20 mA
	Always-On Support Circuitry	75 mA	
Power Dissipated	Single RX Down Convert EN	2.7 W	0.6 W
	Single RX Feed Through	1.7 W	0.7 W
	Single RX Low Power Mode*	0.2 W	0.1 W
	Single RX Sleep Mode**	0.6 W	0.1 W
	TX Up Convert EN	2.2 W	0.7 W
	TX Feed Through	1.3 W	0.7 W
	TX Low Power Mode*	1.3 W	0.1 W
	TX Sleep Mode**	0.2 W	0.1 W
	Always-On Support Circuitry	0.3 W	

Notes for this table are on the next page.

***Note:** When in low power mode, both RF paths, down/up convert and feed through, are disabled. PLL and FPGA remain on for quick recovery to active channel, max 10µs.

****Note:** When in sleep mode, both RF paths, down/up convert and feed through, and the PLL are disabled. Once in sleep mode, it will take 10ms after leaving sleep mode until commands can be sent to PLL and tuner is active again. Current behavior is that when a command is sent to tune to a new frequency the channel will leave sleep mode.

*****Note:** To get the full current/power dissipated for the AM9024 unit, determine the state of each channel, look up the appropriate current/power dissipation for that state, then add current/power draw for each channel together with the "Always-On Support Circuitry" current/power draw. For example: with two RX in down convert and two in low power mode and the TX in sleep mode the current draw on the +3.6V input would be (2 * 740mA) + (2 * 480mA) + 40mA + 75mA = 2.56A corresponding to 9.2W. A similar method would be followed for the +5.5V line then added to the +3.6V numbers to determine total power consumption.

RF CHARACTERISTICS

(T = 25 °C unless otherwise specified)

Parameter	Notes	Min	Typical	Max
Frequency Range	Receive Channel	6 GHz		18 GHz
	Transmit Channel	6 GHz		18 GHz
	Rx/Tx Feedthrough	10 MHz		6 GHz
Bandwidth			1000 MHz	
IF Center Frequency	Receive/Transmit		3 GHz	
Tune Frequency Range	Receive Channel	6 GHz		17.5 GHz
	Transmit Channel	6 GHz		17.5 GHz
	Rx/Tx Feedthrough***	650 MHz		5.975 GHz
Tuning Step Size			25 MHz	
Frequency Reference*	Input Frequency		100 MHz	
	Peak to Peak Input Voltage (VPP)	0.15 V		1.3 V
	Common Mode Input Voltage (VCM)	0.5 V	1.65 V	2.45 V
Tuning Speed			300 µs	
Phase Noise	1 kHz Offset		-90 dBc/Hz	
	10 kHz Offset		-100 dBc/Hz	
	100 kHz Offset		-100 dBc/Hz	
	1 MHz Offset		-118 dBc/Hz	
	10 MHz Offset		-132 dBc/Hz	
Channel to Channel Isolation**	Top CH to Bottom CH; IF Outputs Adjacent		-50 dB	
	Adjacent Channels; IF Outputs "Far" Away		-60 dB	
LO Leakage Channel to Channel	LO @ Input/Output from Other Channels		-80dBm	

***Note:** Reference input may be LVPECL, LVDS, LVHSTL, SSTL, HCSL, or sinusoidal input.

****Note:** Top channel to bottom channel isolation measured by inputting a signal into RX4 and measuring on RX2. Adjacent channel isolation measured by inputting a signal into RX1 and measuring on RX2.

*****Note:** Tune frequencies below 1.5 GHz will all yield the 2 GHz LPF filter path.

RF CHARACTERISTICS (CONTINUED)

(T = 25 °C unless otherwise specified)

Parameter	Notes	Min	Typical	Max
Receive Channels				
Input IP3			+5dBm	
Input IP2			+50 dBm	
Noise Figure			9 dB	12 dB
Image Rejection			80 dB	
LO Radiation			-80 dBm	
Gain		2 dB	5 dB	8 dB
Passband Flatness			+/- 2.5 dB	
Gain Control*			15 dB	
Transmit Channel				
Output IP3			+24 dBm	
Image Rejection			80 dBc	
LO Radiation			-50 dBm	
Harmonics			-70dBc	
Gain		2 dB	5 dB	8 dB
Passband Flatness			+/-3 dB	
Nominal Output Power			0 dBm	
Gain Control*			15 dB	

RF CHARACTERISTICS (CONTINUED)

(T = 25 °C unless otherwise specified)

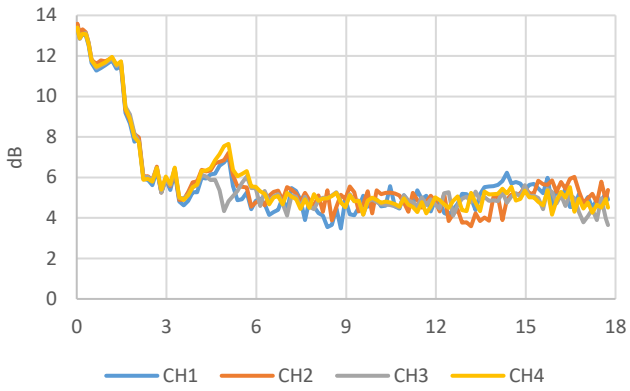
Parameter	Notes	Min	Typical	Max
Receive Feed Through				
Input IP3			+15 dBm	
Noise Figure			5dB	
Gain	Fc < 2.5 GHz	8 dB		11 dB
	2.5 GHz < Fc < 6 GHz	3 dB	5 dB	8 dB
Passband Flatness			+/- 2 dB	
Transmit Feed Through				
Output IP3			+25 dBm	
Harmonics				-50 dBc
Gain	Fc < 2.5 GHz	8 dB		11 dB
	2.5 GHz < Fc < 6 GHz	3 dB	5 dB	8 dB
Passband Flatness			+/- 2 dB	

***Note:** Additional gain control beyond calibrated gain, in 1 dB steps. Down/up convert only.

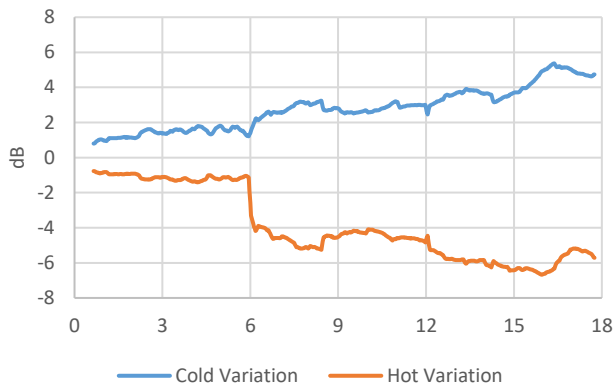
TYPICAL PERFORMANCE

(T = 25 °C and horizontal axis is Frequency in GHz unless otherwise specified. Data representative of a single unit, other units will vary slightly around this data. See provided measured data for each unit for more information.)

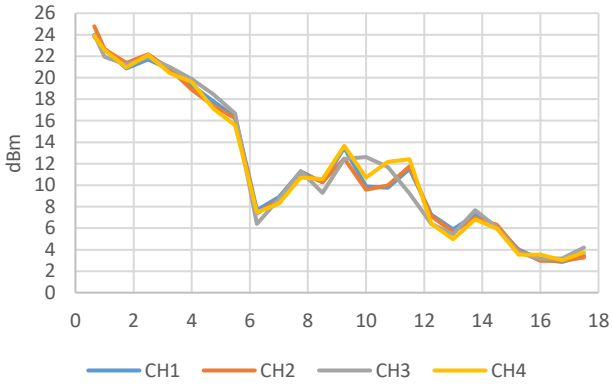
Gain



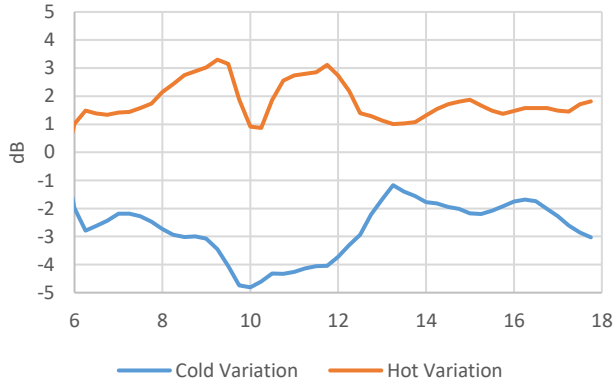
Receive Channel Gain Variation vs Temp*



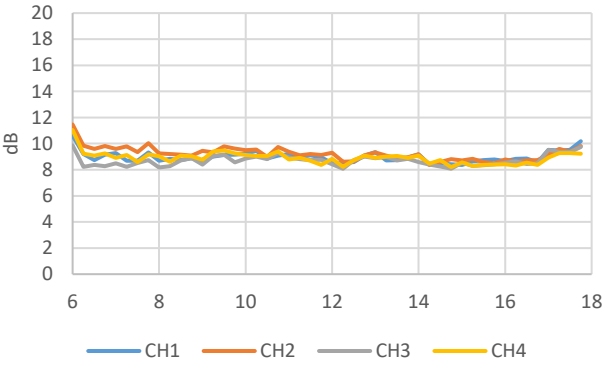
IIP3



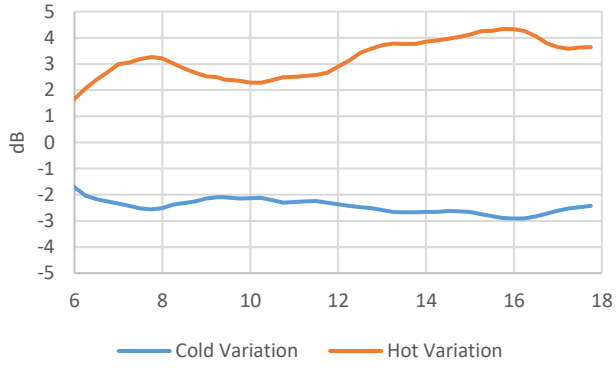
Receive Channel IIP3 Variation vs Temp*



Receive Channel NF



Receive Channel NF Variation vs Temp*

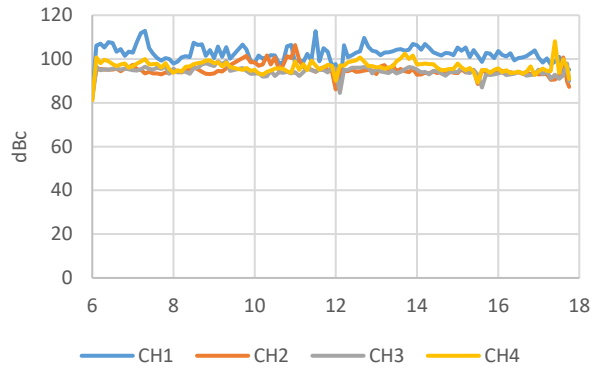


***Note:** Data relative to 25C.

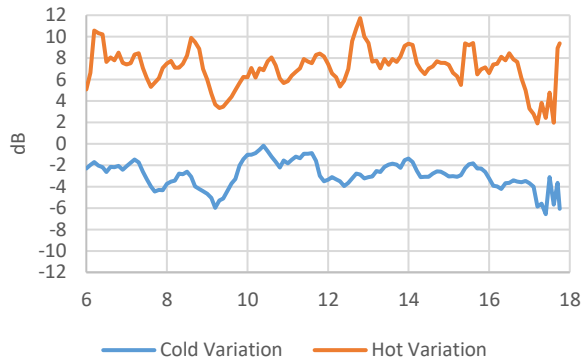
TYPICAL PERFORMANCE (CONTINUED)

(T = 25 °C and horizontal axis is Frequency in GHz unless otherwise specified. Data representative of a single unit, other units will vary slightly around this data. See provided measured data for each unit for more information.)

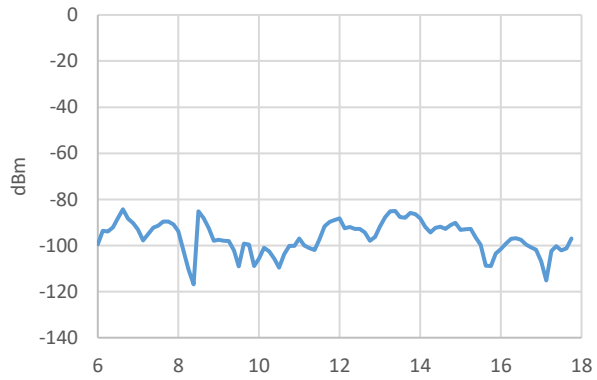
Receive Channel Image Rejection



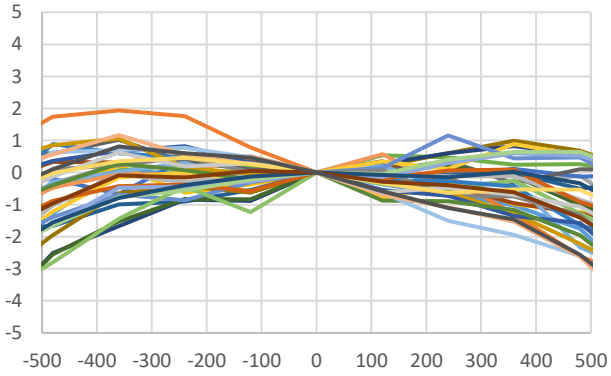
Receive Image Rejection vs Temp



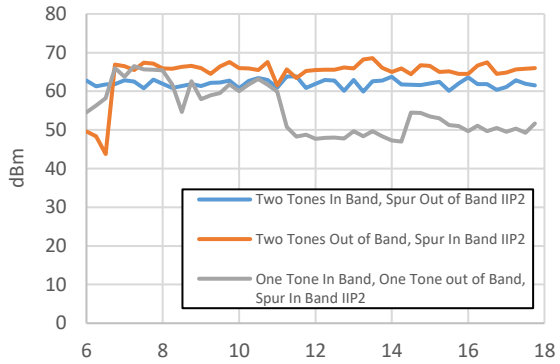
Receive Channel LO Radiation



IF Sweep Relative to Fc (CH4 Shown)**



AM9024 RX IIP2



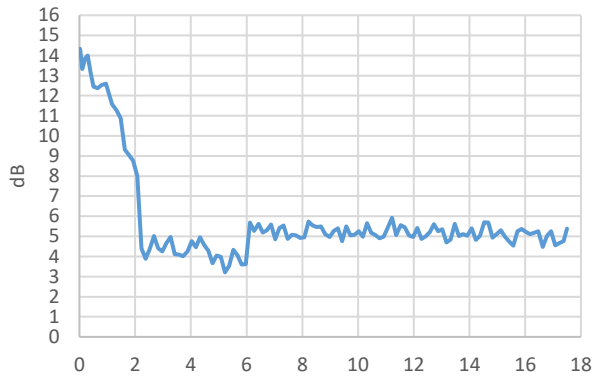
***Note:** Data relative to 25C.

****Note:** Various Fc shown across the down convert range of operation.

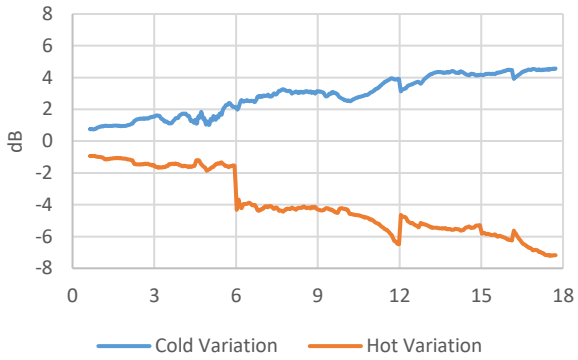
TYPICAL PERFORMANCE (CONTINUED)

(T = 25 °C and horizontal axis is Frequency in GHz unless otherwise specified. Data representative of a single unit, other units will vary slightly around this data. See provided measured data for each unit for more information.)

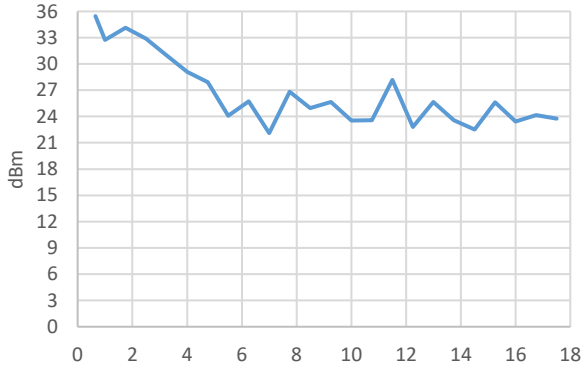
Gain



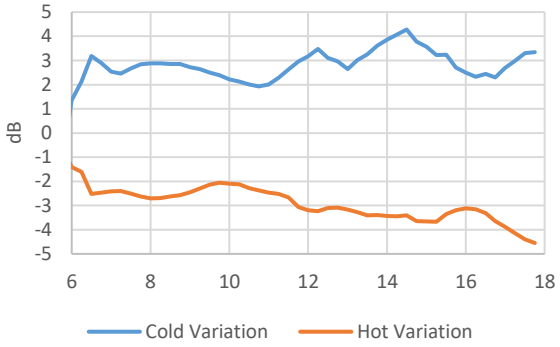
Transmit Channel Gain Variation vs Temp*



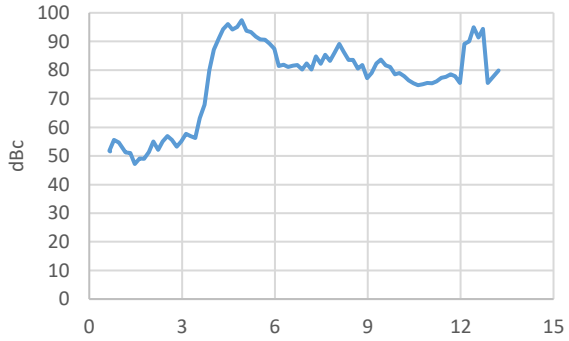
OIP3



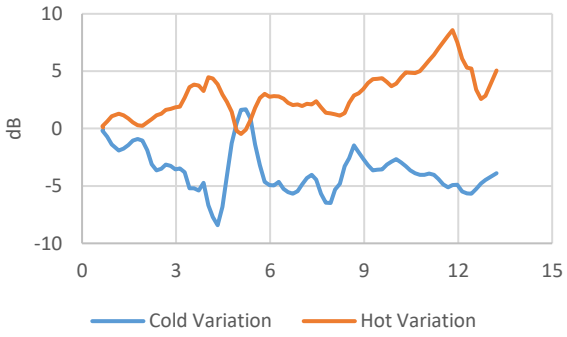
Transmit Channel OIP3 Variation vs Temp*



Transmit Channel HD2**



Transmit Channel HD2 Variation vs Temp*



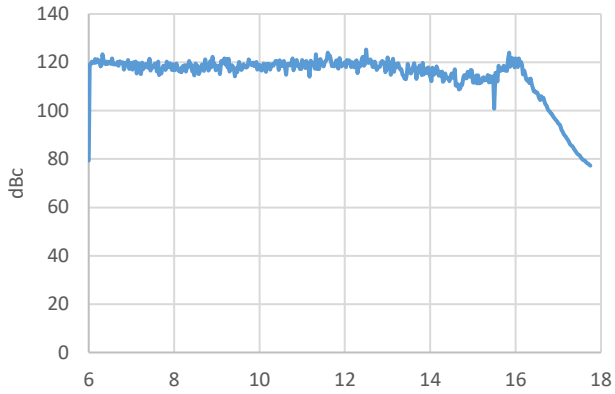
***Note:** Data relative to 25C

****Note:** Measurements taken on a 26.5 GHz spectrum analyzer therefore could only measure to 13.25 GHz Fc. Second harmonic rejection is at a minimum equal if not greater from 13.25 GHz < Fc < 18 GHz therefore ~80dBc should be assumed for HD2 in this range. Measured with a constant -10dBm input power, ~ -5 dBm output power.

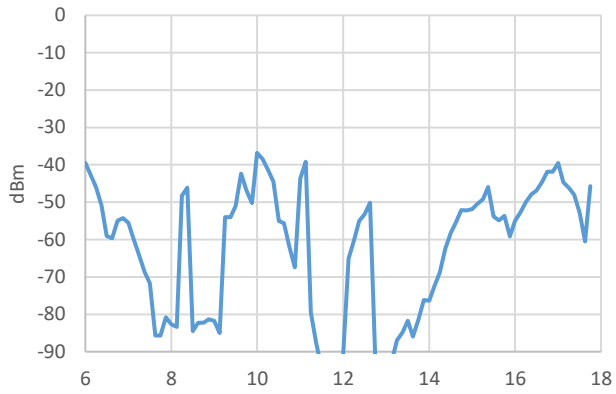
TYPICAL PERFORMANCE (CONTINUED)

(T = 25 °C and horizontal axis is Frequency in GHz unless otherwise specified. Data representative of a single unit, other units will vary slightly around this data. See provided measured data for each unit for more information.)

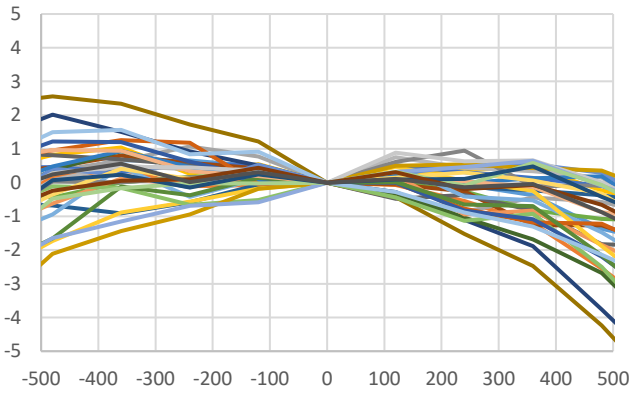
Transmit Channel Image Rejection



LO Radiation



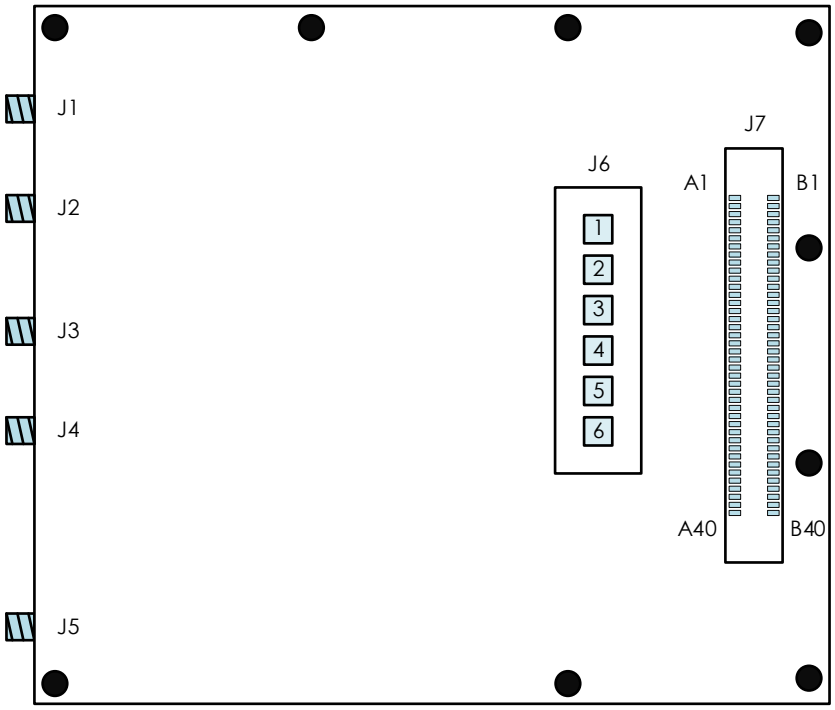
TX IF Sweep Relative to Fc*



***Note:** Various Fc shown across the down convert range of operation.

CONNECTOR AND PIN DEFINITIONS

Board Connector Layout



Connector	Name	Function
J1	RX 3 In	0.4 to 18 GHz RF Input – AC Coupled
J2	RX 2 In	0.4 to 18 GHz RF Input – AC Coupled
J3	RX 4 In	0.4 to 18 GHz RF Input – AC Coupled
J4	RX 1 In	0.4 to 18 GHz RF Input – AC Coupled
J5	TX Out	0.4 to 18 GHz RF Output – AC Coupled
J6	IF In/Out	IF Input/Output Ganged Connector
J7	PWR / CTL	Power and Control Multi-pin Connector

Required Component List

Connector	Mating Connector Part Number	Manufacturer
J1 – J5	52070-006P or 52070-007P	Southwest Microwave
J6	IP5-06-05.0-L-S-1-TR*	Samtec
J7	ERF8-040-05.0-L-DV-L-K-TR	Samtec

Note: Design with footprint compatible for IJ5-06-05.0-L-S-1-TR in the scenario that connectors need to be swapped between host and carrier boards. IJ5 has an extra alignment hole when compared to IP5 footprint.

CONNECTOR PINOUTS

J6 Pin	J6 Pin Name	J6 Pin Function
1	RX2	Receive Channel 2 IF Output – AC Coupled
2	RX4	Receive Channel 4 IF Output – AC Coupled
3	RX1	Receive Channel 1 IF Output – AC Coupled
4	RX3	Receive Channel 3 IF Output – AC Coupled
5	RSRVD	Reserved. Grounded on AM9024
6	TX	Transmit Channel IF Input – AC Coupled

J7 Pin	J7 Pin Name	J7 Pin Function
A1, A4-A8, A24-A28, A33, B1-B8, B24-B28, B33	GND	Ground – Common
A29-A32, B29-B32	+5.5V_IN	+5.5V DC Power Input
A34-A37, B34-B37	+3.6V_IN	+3.6V DC Power Input
A2	REF_P	100 MHz Reference Input, Non-Inverted Input
A3	REF_N	100 MHz Reference Input, Inverted Input
A9	JTAG_TMS	JTAG TMS
A10	JTAG_TCK	JTAG TCK
A11	JTAG_TDI	JTAG TDI
A12	JTAG_TDO	JTAG TDO
A13	SYNC	Tuner LO Sync Line. Use to Sync Phase of RX1 – RX4
A14	MISO	SPI Bus Data Output to Master Controller
A15	SPI_CLK	SPI Bus Clock Input
A16	MOSI	SPI Bus Data Input from Master Controller

J7 Pin	J7 Pin Name	J7 Pin Function
A17	Temp_CSn1	SPI Bus Select Line for Temperature Sensor 1 on Board Top
A18	Temp_CSn2	SPI Bus Select Line for Temperature Sensor 2 on Board Bottom
A19	CMD_CSn1	SPI Bus Select Line to Send Tuner Commands for Receive Channel 1 – Active Low
A20	CMD_CSn2	SPI Bus Select Line to Send Tuner Commands for Receive Channel 2 – Active Low
A21	CMD_CSn3	SPI Bus Select Line to Send Tuner Commands for Receive Channel 3 – Active Low
A22	CMD_CSn4	SPI Bus Select Line to Send Tuner Commands for Receive Channel 4 – Active Low
A23	CMD_CSn5	SPI Bus Select Line to Send Tuner Commands for Transmit Channel – Active Low
B9	Power On_1*	RX1 FPGA Power On Pin – Active High.
B10	Power On_2*	RX2 FPGA Power On Pin – Active High.
B11	Power On_3*	RX3 FPGA Power On Pin – Active High.
B12	Power On_4*	RX4 FPGA Power On Pin – Active High
B13	Power On_5*	TX FPGA Power On Pin – Active High.
B14	LD_1	RX1 Lock Detect – Logic Level High = Locked, Low = Unlocked
B15	LD_2	RX2 Lock Detect – Logic Level High = Locked, Low = Unlocked
B16	LD_3	RX3 Lock Detect – Logic Level High = Locked, Low = Unlocked
B17	LD_4	RX4 Lock Detect – Logic Level High = Locked, Low = Unlocked
B18	LD_5	TX Lock Detect – Logic Level High = Locked, Low = Unlocked
B19	PROG_CSn1	SPI Bus Select Line to Allow On-Board Programming Updates for Receive Channel 1 – Active Low
B20	PROG_CSn2	SPI Bus Select Line to Allow On-Board Programming Updates for Receive Channel 2 – Active Low

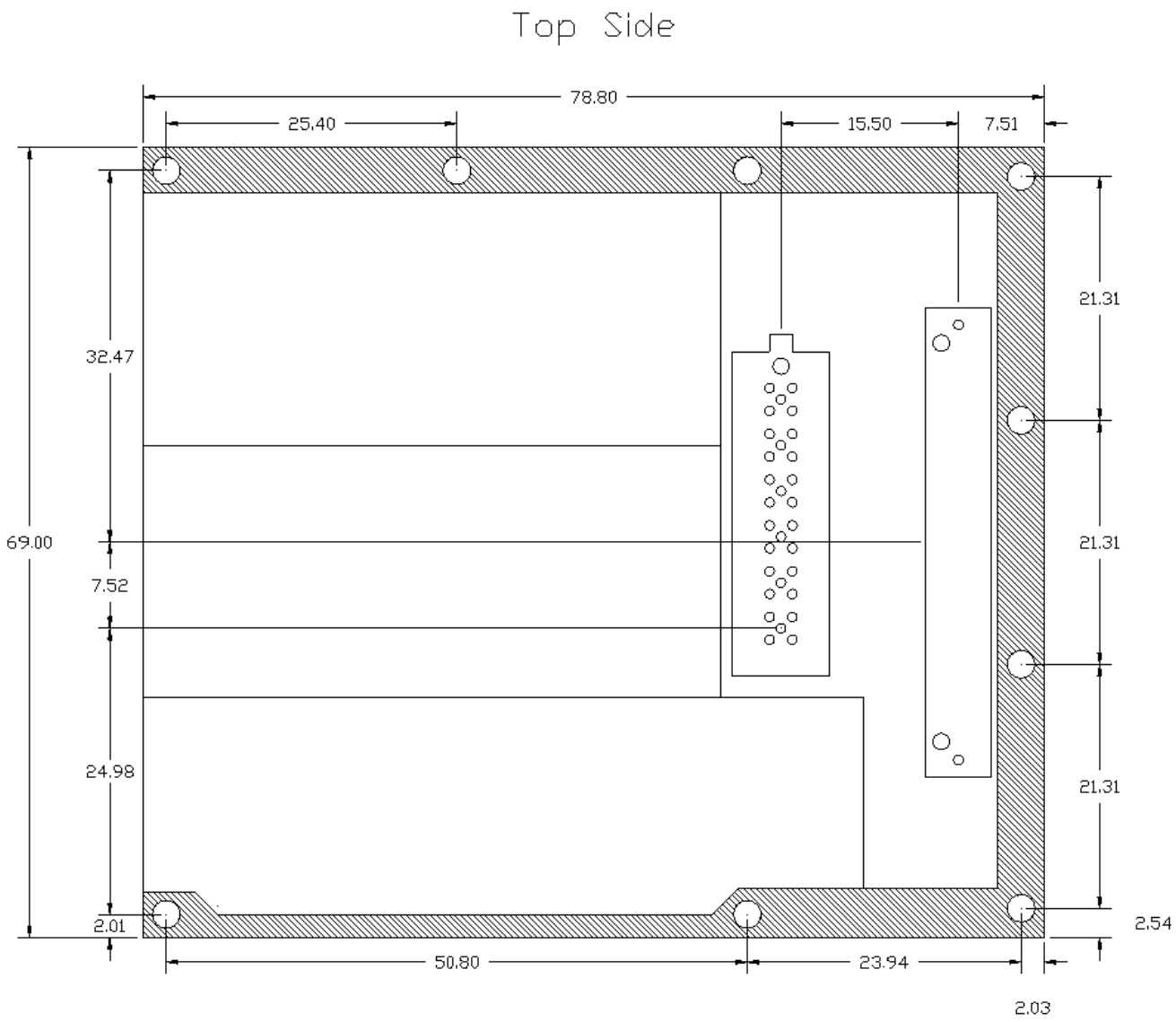
J7 Pin	J7 Pin Name	J7 Pin Function
B21	PROG_CSn3	SPI Bus Select Line to Allow On-Board Programming Updates for Receive Channel 3 – Active Low
B22	PROG_CSn4	SPI Bus Select Line to Allow On-Board Programming Updates for Receive Channel 4 – Active Low
B23	PROG_CSn5	SPI Bus Select Line to Allow On-Board Programming Updates for Transmit Channel – Active Low
A38	RSRVD	Reserved. Connect to +3.6V IN or Leave Floating.
A39	LDO_EN3**	Receive Channel 3 Power Enable – Active High
A40	LDO_EN2**	Receive Channel 2 Power Enable – Active High
B38	LDO_EN5**	Transmit Channel Power Enable – Active High
B39	LDO_EN4**	Receive Channel 4 Power Enable – Active High
B40	LDO_EN1**	Receive Channel 1 Power Enable – Active High

***Note:** When Power On_x is pulled low, FPGA will do a soft reset and then time until tuner channel is active and commands can be sent to the FPGA is approximately 45ms after the pin has been set high. For a hard reset, use "Refresh" command as described in interface control document or toggle LDO_ENx low and then pull high again.

****Note:** Controls entire channel power. If pulled low, all items on that channel will be disabled and you will no longer be able to talk to the FPGA (and JTAG chain will be broken). When turning channel power back on, turn on time is approximately 47ms until commands can be sent to FPGA and tuner is active. If no desire for channel power on/off functionality pin may be tied directly to +3.6V IN. In addition to channel power control, there is power control within a channel while keeping the FPGA and PLL active to reduce time until active, more information is available in provided interface control document.

MECHANICAL DETAILS

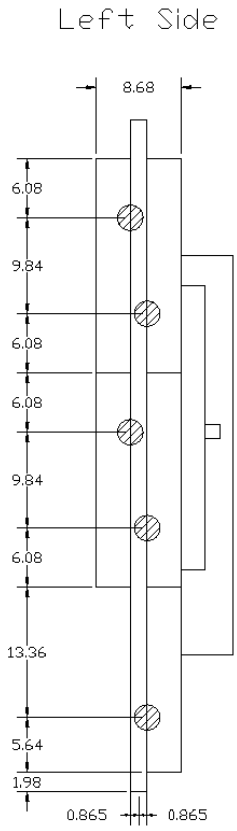
(Dimensions shown are in millimeters unless otherwise specified.)



***Note:** Hatched area denotes exposed metal.
****Note:** Mounting holes around perimeter are sized for a 2-56 screw.

MECHANICAL DETAILS (CONTINUED)

(Dimensions shown are in millimeters unless otherwise specified.)



***Note:** Hatched areas represent edge launch connector.
****Note:** 0.865mm dimension denotes center location of edge launch connector relative to center of PCB, not to be confused for PCB thickness.

Corporate Headquarters

50 Minuteman Road
Andover, MA 01810 USA
+1 978.967.1401 tel
+1 866.627.6951 tel
+1 978.256.3599 fax

International Headquarters
Mercury International
Avenue Eugène-Lance, 38
PO Box 584
CH-1212 Grand-Lancy 1
Geneva, Switzerland
+41 22 884 5100 tel

Learn more
Visit: mrcy.com
For pricing details, contact: MMICsales@mrcy.com
For technical details, contact: MMICsupport@mrcy.com