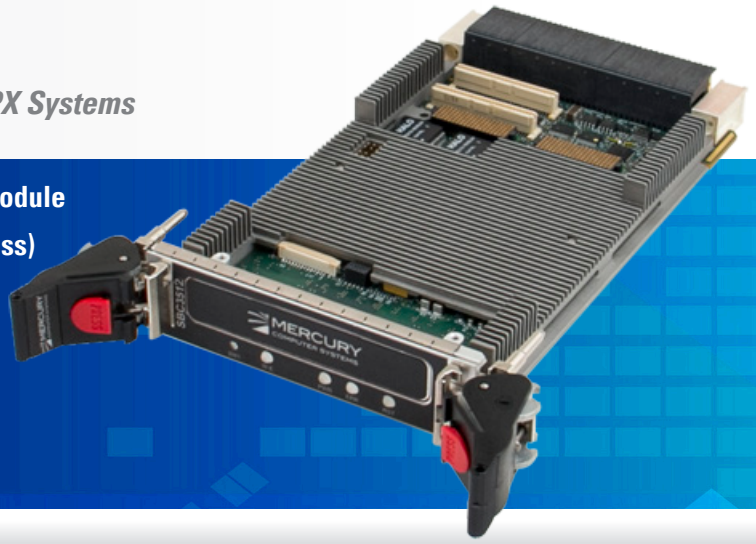
DATASHEET

Ensemble 3000 Series OpenVPX Intel 3rd Generation Core i7 SBC3512 Single Board Computer

MERCURY COMPUTER SYSTEMS™

I/O Optimized SBC-Class Processing for 3U OpenVPX Systems

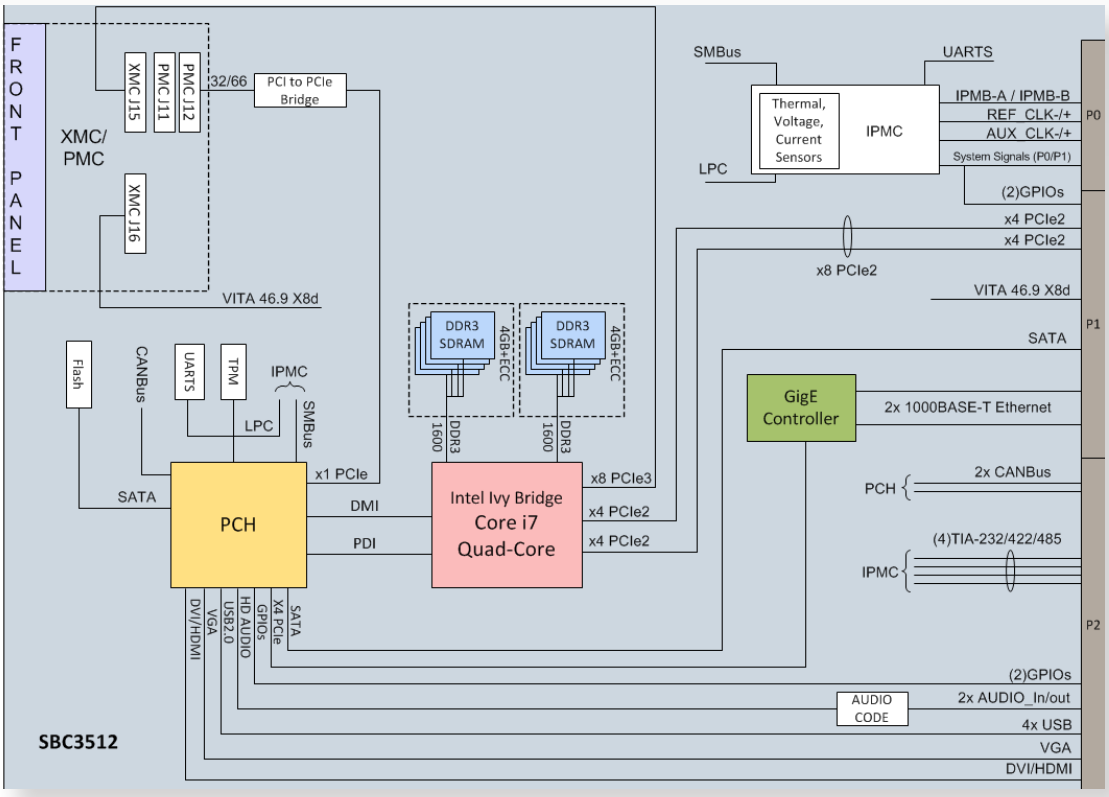


- **3U OpenVPX™-compliant VITA 65/46/48 (VPX-REDI) module**
- **Intel® 3rd Generation Core™ i7 (Ivy Bridge mobile-class) quad-core processor**
- **PMC/XMC Mezzanine Site for Expansion**
- **Built-in SBC-class I/O subsystems**
- **Rugged versions for harsh environments**

The Ensemble® 3000 Series OpenVPX Intel 3rd Generation Core i7 SBC3512 Single-Board Computer from Mercury Computer Systems brings the disruptive compute technology of the Ivy Bridge mobile-class processor to 3U OpenVPX subsystems. Designed with command-and-control applications in mind, the SBC3512 combines the processing capabilities of the processor with significant I/O capabilities. With both built-in I/O and the flexibility of an on-board XMC mezzanine site, the SBC3512 is uniquely suited to meet the intense size, weight and power (SWaP) constraints of the 3U OpenVPX market space.

Intel 3rd Generation Core i7 Ivy Bridge Mobile-Class Processor

The SBC3512 is built on the Intel 64-bit 3rd Generation Core i7 3612QE Ivy Bridge processor, running at up to 2.1 GHz. This processor is based on the Sandy Bridge processor architecture, which includes the revolutionary Intel Advanced Vector Extensions (AVX) instruction set. The AVX instruction set doubles the width of the processor's SIMD engine from 128-bit to 256-bit, delivering a significant improvement in floating point processing capabilities. This architectural advancement results in the SBC3512 delivering approximately 134 peak GFLOPS in the highly constrained 3U OpenVPX form factor.



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The 3612QE processor includes a large 6 MB cache shared between the cores, allowing many high-performance calculations to remain cache resident. This accelerates processing by eliminating the potential latency required to access DRAM to fetch upcoming data. The processor supports dual high-speed DDR3-1600 memory controllers, providing up to 25 GB/s of raw memory bandwidth. Exactly 8 GB of DDR3 SDRAM with ECC support is populated on the SBC3512. The 3612QE processor also includes the entirely redesigned on-chip Intel® GPU, which can be used for HD graphics or GPGPU offload processing if desired.

The Intel Core™ i7 processor supports dual high-speed DDR3 memory controllers. Up to 8 GB of DDR3 SDRAM with ECC support can be populated on the SBC3512.

The SBC3512 makes use of the Panther Point-M Platform Controller Hub (PCH) chipset, which provides integrated graphics capabilities along with I/O bridging between the Intel processor and external devices.

OpenVPX Multiplane Architecture

The SBC3512 is architected to support the multiple physical planes defined by the VITA 65/OpenVPX™ standard. The Data Plane is implemented via a Gen 3 PCI Express® interface connected directly into the Intel Core i7 processor, allowing the SBC3512 to control PCIe® endpoints, such as GPGPU processing modules or FPGA compute modules. From a Control Plane perspective, the SBC3512 implements dual 10/100/1000BASE-T Ethernet interfaces to the backplane to support net-centric applications and networked interconnectivity. Finally, the SBC3512 connects to the Management Plane via dual IPMB interfaces as per the draft VITA 46.11 standard.

Single-Board Computer I/O Capabilities

The SBC3512 includes an extensive array of SBC-class I/O capabilities:

- The inclusion of both DVI/HDMI and legacy VGA graphics interfaces allows the SBC3512 to provide a full graphical display in any configuration, as needed by the application.
- Four TIA-232 serial interfaces are provided to the backplane. Each serial interface can be configured by the user for TIA-232, TIA-422 or TIA-485 signaling.
- Four USB 2.0 interfaces are provided to the backplane for customer use.
- The two SATA interfaces to the backplane easily interface with storage devices.
- Dual CANBus interfaces are available to the backplane to support interfacing with external CANBus systems.
- Dual audio interfaces are provided to the backplane.
- Six GPIO lines act as discrete I/O, usable as input, output or to generate interrupts on the module.
- Several additional bused signals enhance the functionality of the SBC3512 module.

Mezzanine Card Flexibility

The SBC3512 provides a single mezzanine site, able to host both PMC modules and XMC modules. The standard mezzanine site on the SBC3512 module can be configured with off-the-shelf mezzanine cards to bring additional I/O into the system for processing or control, or can host pre-processing elements such as FPGA modules to augment the capabilities of a single 3U OpenVPX slot. PMC cards are supported with a 32-bit PCI™ interface at 33 MHz or 66 MHz on the site. XMCs are supported with x8 PCIe (Gen1 or Gen2) on the J15 connector per the VITA 42.3 standard. Eight differential pairs of XMC user I/O are mapped to the P1 connector for application use.

System Management

The SBC3512 module implements the advanced system management functionality architected in the OpenVPX Specification to enable remote monitoring, alarm management and hardware revision and health status.

Using the standard I2C bus and IPMI protocol, the on-board system-management block implements the Intelligent Platform Management Controller (IPMC) in accordance with the VITA 46.11 draft standard. This allows the SBC3512 module to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal or voltage variations that exceed those thresholds
- Reset the entire module
- Power up/down the entire module
- Retrieve module field replaceable unit (FRU) information
- Be managed remotely by a Chassis Management Controller at the system level, such as implemented on Mercury's 3U OpenVPX switch modules.

VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with a modern high-performance connector set capable of supporting today's high-speed fabric interfaces. VPX is most attractive when paired with the Ruggedized Enhanced Design Implementation standard – REDI (VITA 48). The SBC3512 module is implemented as a 3U conduction-cooled implementation of VPX-REDI, with air-cooled variants in the same VPX form factor available for less rugged environments.

Targeted primarily for harsh-environment embedded applications, VPX-REDI offers extended mechanical configurations supporting higher functional density, such as two-level maintenance (2LM). 2LM allows relatively unskilled maintenance personnel to replace a failed module and restore the system to an operational state in a limited time period, and also minimizes potential damage to the module.

Additional Features

The SBC3512 module provides all the features typically found on a single-board computer. In addition to the sophisticated management subsystem and fabric interconnect, the SBC3512 module provides users with a toolkit enabling many different application use cases.

Features include:

- Real-time clock with granularity to 1 ms and time measurement of up to 30 years
- General-purpose timers for synchronization
- Watchdog timer to support processor interrupt or reset
- Multiple boot paths, include netboot, USB boot and boot from SATA or the on-board flash device

Open Software Environment

Mercury leverages over 25 years of multicomputer software experience, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the SBC3512 module. Because the processor, memory and surrounding technologies are leveraged across product lines, software developed on the SBC3512 module can interface seamlessly with other Mercury products. The same Linux® or VxWorks® development and run-time environment is implemented on the SBC3512 module as on other Intel®-based Mercury platforms across the Ensemble® 3000, 5000 and 6000 Series.

The MultiCore Plus® (MCP) open software environment gives the SBC3512 module access to a wide ecosystem of stacks, middleware, libraries and tools. A key software package available for the SBC3512 module is the MultiCore SAL (MCSAL). MCSAL offers the familiar SAL API interface, but is optimized for the AVX capabilities of the multiple on-chip cores available with the Intel Core™ i7 dual-core processor.

Software support is available on the SBC3512 for the following products:

- Support for Mercury's standard numeric libraries, VSIPL and SAL (Scientific Algorithm Library), as well as their multi-core variants, is optimized for the 2nd Generation Intel Core i7 architecture of the SBC3512 module.
- Open Development Suite for Linux is an Eclipse-based integrated development environment that includes a C/C++ optimizing compiler, a source-level debugger, a language-sensitive text editor, a performance profiler, a project builder, a version control system, a run-time error checker and a graphical source browser. Mercury extensions allow multiprocessor-aware process launch and debug, as well as a System Supervisor view for graphical remote management.

The MultiCore Plus (MCP) software environment lets applications use industry-standard middleware such as uDAPL, DRI, CORBA or standard TCP/IP sockets.

Open Standards Mean Interoperability and Planning for the Future

The OpenVPX™/VITA 65 standard is an industry initiative launched by defense prime contractors and commercial system developers, to take a proactive approach to solving the interoperability issues associated with the VITA 46 (VPX) family of specifications. This group has created an overarching System Specification defining VPX system architecture through pinout definitions to establish a limited set of application-specific reference solutions. These OpenVPX standard solutions provide clear design guidance to suppliers and the user community, assuring interoperability across multi-vendor implementations. The OpenVPX System Specification was ratified by the VSO in February 2010 and ANSI approved as the VITA 65 standard in July 2010.

Specifications

Intel 3rd Generation Core i7 Ivy Bridge Processor

Quad-core with Advanced Vector Extensions (AVX)

2.1 GHz 3612QE

Threads per core 2

Intel Virtualization Technology

DDR3 Up to 8 GB with ECC

Local SATA FLASH

BIOS SPI flash

IPMI (System Management)

On-board IPMI Controller

Voltage and temperature monitor

Geographical address monitor

Power/reset control

On-board FRU EEPROM interface

CPU and CPLD interfaces

Ethernet Connections

10/100/1000BASE-T Ethernet to P2 connector 2

Accessible via OpenVPX RTM or external chassis interface

Ethernet functions supported by the chipset include:

UDP, TCP, SCTP, ARP, IPv4, IPv6, IEEE1588, flow control, 802.1P (priority), and 802.1Q (VLAN)

OpenVPX Multi-Plane Architecture

System Management via IPMB-A and IPMB-B link on P0 Management Plane

Full x8 or dual x4 PCIe® Gen2 on P1 Data Plane

Dual 10/100/1000BASE-T Ethernet Control Plane

PMC/XMC Site

Mezzanine site 1 PMC/XMC

PMC PCI™ support 32-bit, 33 and 66 MHz

PCI-to-PCIe® bridge

Connects PMC site to on-chip PCI Express®

PCIe XMC site per VITA 42.3

8 differential pairs of XMC user-defined I/O from J16 to backplane

Additional I/O Capabilities

TIA-232 serial interfaces to backplane	2
Configurable for TIA-422 or TIA-485 signaling	
USB 2.0 interfaces to backplane	4
DVI/HDMI interface to backplane	1
VGA interface to backplane	1
SATA interfaces to backplane	2
Single-ended GPIO interfaces to backplane	6
CANbus interfaces to backplane	2
Audio interfaces to backplane	2

System signals to backplane

NVMRO, ChassisTest, Environmental Bypass, MemoryClear

Mechanical

3U VPX (air-cooled and conduction-cooled)

1.0" slot pitch

OpenVPX™ and VPX-REDI

Environmental

Air-Cooled – Commercial

Temperature	
Operating	0°C to 40°C*
Storage	-40°C to +85°C
*Customer must maintain required cfm level.	
Humidity	
Operating	10-95%, non-condensing
Vibration	0.003 g2/Hz; 20-2000 Hz, 1 hr/axis
Shock	20g, z-axis; 32g, x-, y-axes; 11 ms half-sine pulse
Altitude	
Operating	0-10,000 ft*
*Customer must maintain required cfm level.	

Air-Cooled – Mercury Rugged Level 1

Temperature	
Operating*	-25°C to +55°C
Storage	-55°C to +85°C
*Customer must maintain required cfm level.	
Humidity	
Operating	5-95%, non-condensing
Vibration	0.04 g2/Hz; 20 to 2000 Hz, 1 hr/axis
Shock	50g, z-axis; 80g, x-, y-axes; 11 ms half-sine
Altitude	
Operating*	0-30,000 ft
*Customer must maintain required cfm level.	

Conduction-Cooled – Mercury Rugged Level 3

Temperature	
Operating	-40°C to +71°C at the card edge*
Storage	-55°C to +125°C
*Customer chassis must maintain card edge at 71°C.	
Humidity	
Operating	0-100%
Vibration	0.1 g2/Hz, based on 5-2000 Hz, 1 hr/axi
Shock	50g, z-axis; 80g, x-, y-axes; 11 ms half-sine
Altitude	
Operating	0-70,000 ft

Compliance

OpenVPX System Specification encompasses

VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11

Compatible with VITA 65

VITA 48/48.1/48.2 (REDI)

PCI Express

Ensemble®

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INNOVATION THAT MATTERS™

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