8Mx64 NOR Flash 3.3V Page Mode Multi-Chip Package

W78M64VP-XSBX

FEATURES

- Access Times of 110, 120ns
- Packaging
  - 159 PBGA, 13x22mm – 1.27mm pitch
- Page Mode
  - Page size is 8 words: Fast page read access from random locations within the page.
- Uniform Sector Architecture
  - One hundred twenty-eight 64 kword
- Single power supply operation
  - 3 volt read, erase, and program operations
- I/O Control
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input.
- Write operation status bits indicate program and erase operation completion
- Suspend and Resume commands for program and erase operations
- Hardware Reset# input resets device
- WP#/ACC Input
  - Accelerates programming time for greater throughput.
  - Protects first and last sector regardless of sector protection settings
- Secured Silicon Sector region
  - 128-word sector for permanent, secure identification through an 8-word random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked at the factory or by the customer
- 100,000 erase cycles per sector typical
- 20-year data retention typical

* This product is subject to change without notice.

GENERAL DESCRIPTION

The W78M64VP-XSBX is a 512Mb, 3.3 volt-only Page Mode memory device.

The device offers fast page access times allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CS#), write enable (WE#) and output enable (OE#) controls.

The device offers uniform 64 Kword (128Kb) Sectors:

Page Mode Features

The page size is 8 words. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.

Standard Flash Memory Features

The device requires a 3.3 volt power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations Page Mode Features

Device Operations

This section describes the read, program, erase, handshaking, and reset features of the Flash devices. Operations are initiated by writing specific commands or a sequence with specific address and data patterns into the command registers (see Table 38 and Table 39). The command register itself does not occupy andy addressable memory location; rather, it is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serves as input to the internal state machine and the state machine outputs dictate the function of the device. Writing incorrect address and data values or writing them in an improper sequence may place the device in an unknown state, in which case the system must pull the RESET# pin low or power cycle the device to return the device to the reading array data mode.

Device Operation Table

The device must be setup appropriately for each operation. Table 2 describes the required state of each control pin for any particular operation.

Read

All memories require access time to output array data. In a read operation, data is read from one memory location at a time. Addresses are presented to the device in random order, and the propagation delay through the device causes the data on its outputs to arrive with the address on its inputs.

The device defaults to reading array data after device power-up or hardware reset. To read data from the memory array, the system must first assert a valid address on A22-A0, while driving OE# and CE# to V_{IL}. WE# must remain at V_{IH}. All addresses are latched on the falling edge of CE#. Data will appear on DQ15-DQ0 after address access time (t_{ACC}), which is equal to the delay from stable addresses to valid output data.

The OE# signal must be driven to V_{IL}. Data is output on DQ15-DQ0 pins after the access time (t_{OE}) has elapsed from the falling edge of OE#, assuming the t_{ACC} access time has been meet.

Page Read Mode

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 words. The appropriate page is selected by the higher address bits A(22)-A3.

FIGURE 1 – PIN CONFIGURATION FOR W78M64VP-XSBX (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10
A		GND	GND	GND	V_{CC}	V_{IO}	GND	GND	GND	V_{CC}
B	V_{IO}	GND	DQ41	WE_3#	V_{IO}	DQ57	DNU	WE_4#	V_{CC}	V_{IO}
C	V_{CC}	DQ33	DQ43	DQ45	DQ47	DQ49	DQ59	DQ61	DQ63	V_{CC}
D	V_{IO}	DQ40	DQ35	DQ37	DQ39	DQ56	DQ51	DQ53	DQ55	V_{IO}
E	V_{CC}	DQ32	DQ42	DQ44	DQ46	DQ48	DQ58	DQ60	DQ62	V_{CC}
F	GND	CS_3#	DQ34	DQ36	DQ38	CS_4#	DQ50	DQ52	DQ54	GND
G	GND	OE#	A0	A22	V_{CC}	A12	A16	A21	A20	GND
H	GND	A2	WP#/A_{CC}	A11	GND	V_{IO}	A7	A10	A15	GND
J	GND	A3	A6	A9	V_{CC}	GND	A1	RESET#	A13	GND
K	GND	A4	A17	RY/BY#	GND	A14	A5	A18	A8	GND
L	GND	DQ_{17}	WE_2#	DQ29	DNU*	DQ9	DQ4	WE_1#	A19	GND
M	V_{IO}	DQ24	DQ19	DQ21	DQ31	DQ1	DQ11	DQ6	DQ15	V_{IO}
N	V_{CC}	DQ16	DQ26	DQ28	DQ23	DQ8	DQ3	DQ13	DQ7	V_{CC}
P	V_{IO}	CS2#	DQ18	DQ20	DQ30	DQ0	DQ10	DQ5	DQ14	V_{IO}
R	V_{CC}	V_{CC}	DQ25	DQ27	DQ22	CS_1#	DQ2	DQ12	GND	V_{CC}
T	V_{IO}	GND	GND	GND	V_{IO}	V_{CC}	GND	GND	GND	V_{IO}

* Ball L5 is reserved for A23 for future upgrades.

Address bits A2-A0 in word mode determine the specific word within a page. The microprocessor supplies the specific word location. The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{ACC}. When CE# is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the “read-page addresses” constant and changing the “intra-read page” addresses.

Autoselect

The Autoselect mode provides manufacturer ID, Device identification, and sector protection information, through identifier codes output from the internal register (separate from the memory array) on DQ7-DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm (see

FIGURE 2 – PIN DESCRIPTION

DQ_{0-63}	Data Inputs/Outputs
A_{0-22}	Address Inputs
$WE\#_{1-4}$	Write Enables
$CS\#_{1-4}$	Chip Selects
OE#	Output Enable
RESET#	Hardware Reset
WP#/ACC	Hardware Write Protection/Acceleration
RY/BY#	Ready/Busy Output
V_{CC}	Power Supply
V_{IO}	Versatile I/O Input
GND	Ground
DNU	Do Not Use

FIGURE 3 – BLOCK DIAGRAM

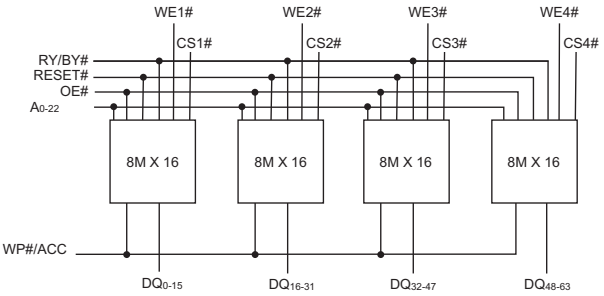


Table 4). The Autoselect codes can also be accessed in-system.

There are two methods to access autoselect codes. One uses the autoselect command, the other applies V_{ID} on address pin A9.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins must be as shown in Table 3.

- To access Autoselect mode without using high voltage on A9, the host system must issue the Autoselect command.
- The Autoselect command sequence may be written to an address within a sector that is either in the read or erase-suspend-read mode.
- The Autoselect command may not be written while the device is actively programming or erasing.
- The system must write the reset command to return to the read mode (or erase-suspend-read mode if the sector was previously in Erase Suspend).
- It is recommended that A9 apply V_{ID} after power-up sequence is completed. In addition, it is recommended that A9 apply from V_{ID} to V_{IH}/V_{IL} before power-down the V_{CC}/V_{IO}.
- See Table 39 for command sequence details.

- When verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 5 to Table 6). The remaining address bits are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15-DQ0. The Autoselect codes can also be accessed in-system through the command register.

Program/Erase Operations

These devices are capable of several modes of programming and or erase operations which are described in detail in the following sections.

During a write operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing address, command, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#.

The Unlock Bypass feature allows the host system to send program commands to the Flash device without first writing unlock cycles within the command sequence. See Unlock Bypass section for details on the Unlock Bypass function.

Note the following:

- When the Embedded Program algorithm is complete, the device returns to the read mode.
- The system can determine the status of the program operation by reading the DQ status bits. Refer to the Write Operation Status for information on these status bits.
- An “0” cannot be programmed back to a “1.” A succeeding read shows that the data is still “0.”
- Only erase operations can convert a “0” to a “1.”
- Any commands written to the device during the Embedded Program/Erase are ignored except the Suspend commands.
- Secured Silicon Sector, Autoselect, and CFI functions are unavailable when a program operation is in progress.
- A hardware reset and/or power removal immediately terminates the Program/Erase operation and the
- Program/Erase command sequence should be reinitiated once the device has returned to the read mode to ensure data integrity.
- Programming is allowed in any sequence and across sector boundaries for single word programming operation. See Write Buffer Programming when using the write buffer.
- Programming to the same word address multiple times without intervening erases is permitted.

Single Word Programming

Single word programming mode is one method of programming the Flash. In this mode, four Flash command write cycles are used to program an individual Flash address. The data for this programming operation could be 8 or 16-bits wide.

While the single word programming method is supported by most Spansion devices, in general Single Word Programming is not recommended for devices that support Write Buffer Programming. See Table 38 for the required bus cycles and Figure 4 for the flowchart. When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by reading the DQ status bits. Refer to Write Operation Status for information on these status bits.

- During programming, any command (except the Suspend Program command) is ignored.
- The Secured Silicon Sector, Autoselect, and CFI functions are unavailable when a program operation is inprogress.
- A hardware reset immediately terminates the program operation. The program command sequence should
- be reinitiated once the device has returned to the read mode, to ensure data integrity.
- Programming to the same address multiple times continuously (for example, “walking” a bit within a word) is permitted.

Write Buffer Programming

Write Buffer Programming allows the system to write a maximum of 32 words in one programming operation. This results in a faster effective word programming time than the standard “word” programming algorithms.

The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming occurs. At this point, the system writes the number of “word locations minus 1” that are loaded into the page buffer at the Sector Address in which programming occurs. This tells the device how many write buffer addresses are loaded with data and therefore when to expect the “Program Buffer to Flash” confirm command. The number of locations to program cannot exceed the size of the write buffer or the operation aborts. (Number loaded = the number of locations to program minus 1. For example, if the system programs 6 address locations, then 05h should be written to the device.)

The system then writes the starting address/data combination. This starting address is the first address/data pair to be programmed, and selects the “write-buffer-page” address. All subsequent address/data pairs must fall within the elected-write-buffer-page.

The “write-buffer-page” is selected by using the addresses AMAX–A5.

The “write-buffer-page” addresses must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple “write-buffer-pages.” This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected “write-buffer-page”, the operation ABORTs.)

After writing the Starting Address/Data pair, the system then writes the remaining address/data pairs into the write buffer.

Note that if a Write Buffer address location is loaded multiple times, the “address/data pair” counter is decremented for every data load operation. Also, the last data loaded at a location before the “Program Buffer to Flash” confirm command is the data programmed into the device. It is the software's responsibility to comprehend ramifications of loading a write-buffer location more than once. The counter decrements for each data load operation, NOT for each unique write-buffer-address location. Once the specified number of write buffer locations have been loaded, the system must then write the “Program Buffer to Flash” command at the Sector Address. Any other address/data write combinations abort the Write Buffer Programming operation. The Write Operation Status bits should be used while monitoring the last address location loaded into the write buffer. This eliminates the need to store an address in memory because the system can load the last address location, issue the program confirm command at the last loaded address location, and then check the write operation status at that same address. DQ7, DQ6, DQ5, DQ2, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer “embedded” programming operation can be suspended using the standard suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device returns to READ mode. The Write Buffer Programming Sequence is ABORTED under any of the following conditions:

- Load a value that is greater than the page buffer size during the “Number of Locations to Program” step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the “Starting Address” during the “write buffer data loading” stage of the operation.
- Writing anything other than the Program to Buffer Flash Command after the specified number of “data load” cycles.
- The ABORT condition is indicated by DQ1 = 1, DQ7 = DATA# (for the “last address location loaded”), DQ6 = TOGGLE, DQ5 = 0. This indicates that the Write Buffer Programming Operation was ABORTED. A “Write-to- Buffer-Abort reset” command sequence is required when using the write buffer Programming features in Unlock Bypass mode. Note that the Secured Silicon sector, autoselect, and CFI functions are unavailable when a program operation is in progress.

Write buffer programming is allowed in any sequence of memory (or address) locations. These flash devices are capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases.

Use of the write buffer is strongly recommended for programming when multiple words are to be programmed.

Sector Erase

The sector erase function erases one or more sectors in the memory array. (See Table 38 and Figure 6.) The device does not require the system to preprogram a sector prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory to an all zero data pattern prior to electrical erase. After a successful sector erase, all locations within the erased sector contain FFFFh. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than t_{SEA} occurs. During the timeout period, additional sector addresses may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs. Any sector erase address and command following the exceeded time-out (50µs) may or may not be accepted. Any command other than Sector Erase or Erase Suspend during the time-out period resets that sector to the read mode. The system can monitor DQ3 to determine if the sector erase timer has timed out. The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the sector returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7 or DQ6/DQ2 in the erasing sector. Refer to Section write operation status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that sector has returned to reading array data, to ensure the sector is properly erased.

The Unlock Bypass feature allows the host system to send program commands to the Flash device without first writing unlock cycles within the command sequence. See Unlock Bypass Section for details on the Unlock Bypass function.

Figure 6 illustrates the algorithm for the erase operation. Refer to Erase and Programming Performance Section for parameters and timing diagrams.

Chip Erase Command Sequence

Chip erase is a six-bus cycle operation as indicated by Table 39. These commands invoke the Embedded Erase algorithm, which does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory to an all zero data pattern prior to electrical erase. After a successful chip erase, all locations of the chip contain FFFFh. The system is not required to provide any controls or timings during these operations. The Command Definitions shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that sector returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. Refer to “Write Operation Status” for information on these status bits.

The Unlock Bypass feature allows the host system to send program commands to the Flash device without first writing unlock cycles within the command sequence. See Unlock Bypass Section for details on the Unlock Bypass function.

Any commands written during the chip erase operation are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that sector has returned to reading array data, to ensure the entire array is properly erased.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The sector address is required when writing this command. This command is valid only during the sector erase operation, including the minimum t_{SEA} time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 µs (5 µs typical) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7-DQ0. The system can use DQ7, or DQ6, and DQ2 together, to determine if a sector is actively erasing or is erase-suspended.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using write operation status bits, just as in the standard program operation.

In the erase-suspend-read mode, the system can also issue the Autoselect command sequence. Refer to Write Buffer Programming Section and the Autoselect Section.

To resume the sector erase operation, the system must write the Erase Resume command. The address of the erase-suspended sector is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Program Suspend/Program Resume Commands

The Program Suspend command allows the system to interrupt an embedded programming operation or a “Write to Buffer” programming operation so that data can read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the programming operation within 15 µs maximum (5 µs typical) and updates the status bits. Addresses are “don't-cares” when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any nonsuspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not within a sector in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area, then user must use the proper command sequences to enter and exit this region.

The system may also write the Autoselect Command Sequence when the device is in Program Suspend

mode. The device allows reading Autoselect codes in the suspended sectors, since the codes are not stored in the memory array. When the device exits the Autoselect mode, the device reverts to Program Suspend mode, and is ready for another valid operation. See Autoselect Section.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the write operation status bits, just as in the standard program operation. See Write Operation Status Section for more information.

The system must write the Program Resume command (address bits are “don't care”) to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resumed programming.

Accelerated Program

Accelerated single word programming and write buffer programming operations are enabled through the WP#/ACC pin. This method is faster than the standard program command sequences.

Note

The accelerated program functions must not be used more than 10 times per sector. If the system asserts VHH on this input, the device automatically enters the aforementioned Unlock Bypass mode and uses the higher voltage on the input to reduce the time required for program operations. The system can then use the Write Buffer Load command sequence provided by the Unlock Bypass mode. Note that if a “Write-to-Buffer-Abort Reset” is required while in Unlock Bypass mode, the full 3-cycle RESET command sequence must be used to reset the device. Removing V_{HH} from the ACC input, upon completion of the embedded program operation, returns the device to normal operation.

- Sectors must be unlocked prior to raising WP#/ACC to V_{HH}.
- The WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result.
- It is recommended that WP#/ACC apply V_{HH} after power-up sequence is completed. In addition, it is recommended that WP#/ACC apply from V_{HH} to V_{IH}/V_{IL} before powering down V_{CC}/V_{IO}.

UNLOCK BYPASS

This device features an Unlock Bypass mode to facilitate shorter programming commands. Once the device enters the Unlock Bypass mode, only two write cycles are required to program data, instead of the normal four cycles.

This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. The Command Definitions shows the requirements for the unlock bypass command sequences.

During the unlock bypass mode, only the Read, Program, Write Buffer Programming, Write-to-Buffer-Abort Reset, and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the sector address and the data 90h. The second cycle need only contain the data 00h. The sector then returns to the read mode.

Write Operation Status

The device provides several bits to determine the status of a program or erase operation. The following subsections describe the function of DQ1, DQ2, DQ3, DQ5, DQ6, and DQ7.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence. Note that the Data# Polling is valid only for the last word being programmed in the write-buffer-page during Write Buffer Programming. Reading Data# Polling status on any word other than the last word to be programmed in the write-buffer-page returns false status information.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# polling on DQ7 is active, then that sector returns to the read mode.

During the Embedded Erase Algorithm, Data# polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6-DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6-DQ0 may be still invalid. Valid data on DQ7-D00 appears on successive read cycles.

See the following for more information: Table 18, shows the outputs for Data# Polling on DQ7. Figure 7, shows the Data# Polling algorithm; and Figure 22, shows the Data# Polling timing diagram.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address that is being programmed or erased causes DQ6 to toggle. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program Algorithm is complete.

Toggle Bit I on DQ6 requires either OE# or CE# to be de-asserted and reasserted to show the change in state.

DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 18 to compare outputs for DQ2 and DQ6.

Reading Toggle Bits DQ6/DQ2

Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store

the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erases operation. The system can read array data on DQ7–DQ0 on the following read cycle. However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see DQ5: Exceeded Timing Limits). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erases operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data. The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. Refer to Figure 7 for more details.

NOTE

When verifying the status of a write operation (embedded program/erase) of a memory sector, DQ6 and DQ2 toggle between high and low states in a series of consecutive and contiguous status read cycles. In order for this toggling behavior to be properly observed, the consecutive status bit reads must not be interleaved with read accesses to other memory sectors. If it is not possible to temporarily prevent reads to other memory sectors, then it is recommended to use the DQ7 status bit as the alternative method of determining the active or inactive status of the write operation.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed. The device does not output a 1 on DQ5 if the system tries to program a 1 to a location that was previously programmed to 0. Only an erase operation can change a 0 back to a 1. Under this condition, the device ignores the bit that was incorrectly instructed to be programmed from a 0 to a 1, while any other bits that were correctly requested to be changed from 1 to 0 are programmed. Attempting to program a 0 to a 1 is masked during the programming operation. Under valid DQ5 conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a sector was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timeout State Indicator

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” If the time between additional sector erase commands from the system can be assumed to be less than t_{SEA}, then the system need not monitor DQ3. See Sector Erase for more details.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device accepts additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each sub-sequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 18 shows the status of DQ3 relative to the other status bits.

DQ1: Write to Buffer Abort

DQ1 indicates whether a Write to Buffer operation was aborted. Under these conditions DQ1 produces a “1”. The system must issue the “Write to Buffer Abort Reset” command sequence to return the device to reading array data. See Write Buffer Programming for more details.

Writing Commands/Command Sequences

During a write operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing an address, command, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#. An erase operation can erase one sector, multiple sectors, or the entire device. Table 1 indicate the address space that each sector occupies. The device address space is divided into uniform 64KW/128KB sectors. A sector address is the set of address bits required to uniquely select a sector. $I_{CC}2$ in “DC Characteristics” represents the active current specification for the write mode. “AC Characteristics” contains timing specification tables and timing diagrams for write operations.

RY/BY#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to VCC. This feature allows the host system to detect when data is ready to be read by simply monitoring the RY/BY# pin, which is a dedicated output and controlled by CE# (not OE#).

Hardware Reset

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP} (RESET# Pulse Width), the device immediately terminates any operation in progress, tristates all outputs, resets the configuration register, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data.

To ensure data integrity Program/Erase operations that were interrupted should be reinitiated once the device is ready to accept another command sequence.

When RESET# is held at V_{SS}, the device draws V_{CC} reset current ($I_{CC}5$). If RESET# is held at V_{IL}, but not at V_{SS}, the standby current is greater. RESET# may be tied to the system reset circuitry which enables the system to read the boot-up firmware from the Flash memory upon a system reset.

Software Reset

Software reset is part of the command set (see Table 12.1 on page 69) that also returns the device to arrayread mode and must be used for the following conditions:

1. to exit Autoselect mode
2. when DQ5 goes high during write status operation that indicates program or erase cycle was not successfully completed
3. exit sector lock/unlock operation.
4. to return to erase-suspend-read mode if the device was previously in Erase Suspend mode.
5. after any aborted operations

The following are additional points to consider when using the reset command:

- This command resets the sectors to the read and address bits are ignored.
- Reset commands are ignored during program and erase operations.
- The reset command may be written between the cycles in a program command sequence before programming begins (prior to the third cycle). This resets the sector to which the system was writing to the read mode.
- If the program command sequence is written to a sector that is in the Erase Suspend mode, writing the reset command returns that sector to the erase-suspend-read mode.
- The reset command may be written during an Autoselect command sequence.
- If a sector has entered the Autoselect mode while in the Erase Suspend mode, writing the reset command returns that sector to the erase-suspend-read mode.
- If DQ1 goes high during a Write Buffer Programming operation, the system must write the “Write to Buffer abort Reset” command sequence to RESET the device to reading array data. The standard RESET command does not work during this condition.
- To exit the unlock bypass mode, the system must issue a two-cycle unlock bypass reset command sequence [see Command Definitions for details].

Advanced Sector Protection/Unprotection

The Advanced Sector Protection/Unprotection feature disables or enables programming or erase operations in any or all sectors and can be implemented through software and/or hardware methods, which are independent of each other. This section describes the various methods of protecting data stored in the memory array. An overview of these methods in shown in Figure 8.

Lock Register

As shipped from the factory, all devices default to the persistent mode when power is applied, and all sectors are unprotected. The device programmer or host system must then choose which sector protection method to use. Programming (setting to “0”) any one of the following two one-time programmable, non-volatile bits locks the part permanently in that mode:

- Lock Register Persistent Protection Mode Lock Bit (DQ1)
- Lock Register Password Protection Mode Lock Bit (DQ2)

NOTES

1. If the password mode is chosen, the password must be programmed before setting the corresponding lock register bit.
2. After the Lock Register Bits Command Set Entry command sequence is written, reads and writes for Sector 0 are disabled, while reads from other sectors are allowed until exiting this mode.
3. If both lock bits are selected to be programmed (to zeros) at the same time, the operation aborts.
4. Once the Password Mode Lock Bit is programmed, the Persistent Mode Lock Bit is permanently disabled, and no changes to the protection scheme are allowed. Similarly, if the Persistent Mode Lock Bit is programmed, the Password Mode is permanently disabled.

After selecting a sector protection method, each sector can operate in any of the following three states:

1. Constantly locked. The selected sectors are protected and can not be reprogrammed unless PPB lock bit is cleared via a password, hardware reset, or power cycle.
2. Dynamically locked. The selected sectors are protected and can be altered via software commands.
3. Unlocked. The sectors are unprotected and can be erased and/or programmed.

Persistent Protection Bits

The Persistent Protection Bits are unique and nonvolatile for each sector and have the same endurances as the Flash memory. Preprogramming and verification prior to erasure are handled by the device, and therefore do not require system monitoring.

NOTES

1. Each PPB is individually programmed and all are erased in parallel.
2. While programming PPB for a sector, array data can be read from any other sector, except Sector 0 (used for Data# Polling) and the sector in which sector PPB is being programmed.
3. Entry command disables reads and writes for the sector selected.
4. Reads within that sector return the PPB status for that sector.
5. All Reads must be performed using the read mode.

6. The specific sector address (A22-A16) are written at the same time as the program command.
7. If the PPB Lock Bit is set, the PPB Program or erase command does not execute and times-out without programming or erasing the PPB.
8. There are no means for individually erasing a specific PPB and no specific sector address is required for this operation.
9. Exit command must be issued after the execution which resets the device to read mode and reenables reads and writes for Sector 0.
10. The programming state of the PPB for a given sector can be verified by writing a PPB Status Read Command to the device as described by the flow chart shown in Figure 9.

Dynamic Protection Bits

Dynamic Protection Bits are volatile and unique for each sector and can be individually modified. DYBs only control the protection scheme for unprotected sectors that have their PPBs cleared (erased to “1”). By issuing the DYB Set or Clear command sequences, the DYBs are set (programmed to “0”) or cleared (erased to “1”), thus placing each sector in the protected or unprotected state respectively. This feature allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed.

NOTES

1. The DYBs can be set (programmed to “0”) or cleared (erased to “1”) as often as needed. When the parts are first shipped, the PPBs are cleared (erased to “1”) and upon power up or reset, the DYBs can be set or cleared depending upon the ordering option chosen.
2. If the option to clear the DYBs after power up is chosen, (erased to “1”), then the sectors may be modified depending upon the PPB state of that sector (see Table 20).
3. The sectors would be in the protected state If the option to set the DYBs after power up is chosen (programmed to “0”).
4. It is possible to have sectors that are persistently locked with sectors that are left in the dynamic state.
5. The DYB Set or Clear commands for the dynamic sectors signify protected or unprotected state of the sectors respectively. However, if there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock Bit must be cleared by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again locks the PPBs, and the device operates normally again.
6. To achieve the best protection, it is recommended to execute the PPB Lock Bit Set command early in the boot code and protect the boot code by holding WP#/ACC = V_{IL}. Note that the PPB and DYB bits have the same function when WP#/ACC = V_{HH} as they do when ACC =V_{IH}.

Persistent Protection Bit Lock Bit

The Persistent Protection Bit Lock Bit is a global volatile bit for all sectors. When set (programmed to “0”), it locks all PPBs and when cleared (programmed to “1”), allows the PPBs to be changed. There is only one PPB Lock Bit per device.

NOTES

1. No software command sequence unlocks this bit unless the device is in the password protection mode; only a hardware reset or a power-up clears this bit.
2. The PPB Lock Bit must be set (programmed to “0”) only after all PPBs are conFigured to the desired settings.

Password Protection Method

The Password Protection Method allows an even higher level of security than the Persistent Sector Protection Mode by requiring a 64-bit password for unlocking the device PPB Lock Bit. In addition to this password requirement, after power up and reset, the PPB Lock Bit is set “0” to maintain the password mode of operation. Successful execution of the Password Unlock command by entering the entire password clears the PPB Lock Bit, allowing for sector PPBs modifications.

NOTES

1. There is no special addressing order required for programming the password. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent access.
2. The Password Program Command is only capable of programming “0”s. Programming a “1” after a cell is programmed as a “0” results in a time-out with the cell as a “0”.
3. The password is all “1”s when shipped from the factory.
4. All 64-bit password combinations are valid as a password.
5. There is no means to verify what the password is after it is set.
6. The Password Mode Lock Bit, once set, prevents reading the 64-bit password on the data bus and further password programming.
7. The Password Mode Lock Bit is not erasable.
8. The lower two address bits (A1–A0) are valid during the Password Read, Password Program, and Password Unlock.
9. The exact password must be entered in order for the unlocking function to occur.
10. The Password Unlock command cannot be issued any faster than 1 µs at a time to prevent a hacker from running through all the 64-bit combinations in an attempt to correctly match a password.
11. Approximately 1 µs is required for unlocking the device after the valid 64-bit password is given to the device.
12. Password verification is only allowed during the password programming operation.
13. All further commands to the password region are disabled and all operations are ignored.

14. If the password is lost after setting the Password Mode Lock Bit, there is no way to clear the PPB Lock Bit.
15. Entry command sequence must be issued prior to any of any operation and it disables reads and writes for Sector 0. Reads and writes for other sectors excluding Sector 0 are allowed.
16. If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode.
17. A program or erase command to a protected sector enables status polling and returns to read mode without having modified the contents of the protected sector.
18. The programming of the DYB, PPB, and PPB Lock for a given sector can be verified by writing individual status read commands DYB Status, PPB Status, and PPB Lock Status to the device.

Hardware Data Protection Methods

The device offers two main types of data protection at the sector level via hardware control:

- When WP#/ACC is at V_{IL}, the either the highest or lowest sector is locked (device specific).

There are additional methods by which intended or accidental erasure of any sectors can be prevented via hardware means. The following subsections describes these methods:

WP#/ACC Method

The Write Protect feature provides a hardware method of protecting one outermost sector. This function is provided by the WP#/ACC pin and overrides the previously discussed Sector Protection/ Unprotection method.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the highest or lowest sector independently of whether the sector was protected or unprotected using the method described in Advanced Sector Protection/ Unprotection.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected.

The WP#/ACC pin must be held stable during a command sequence execution. WP# has an internal pull-up; when unconnected, WP# is set at V_{IH}.

NOTE
If WP#/ACC is at V_{IL} when the device is in the standby mode, the maximum input load current is increased.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when VCC is greater than V_{LKO}.

Write Pulse “Glitch Protection”

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Power-Up Write Inhibit

If WE# = CE# = RESET# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

Power Conservation Modes

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input. The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at V_{CC} ± 0.3 V. The device requires standard access time (t_{CE}) for read access, before it is ready to read data. If the device is deselected during erasure or programming, the device draws active current until the operation is completed. $I_{CC}4$ in “DC Characteristics” represents the standby current specification

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. $I_{CC}6$ represents the automatic sleep mode current specification.

Hardware RESET# Input Operation

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/ write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence to ensure data integrity.

When RESET# is held at V_{SS} ± 0.3 V, the device draws I_{CC} reset current ($I_{CC}5$). If RESET# is held at V_{IL} but not within V_{SS} ± 0.3 V, the standby current is greater.

RESET# may be tied to the system reset circuitry and thus, a system reset would also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Output Disable (OE#)

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state. (With the exception of RY/BY#.)

Secured Silicon Sector Flash Memory Region

Secured Silicon Sector Flash Memory Region The Secured Silicon Sector provides an extra Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is 128 words in length and all Secured Silicon reads outside of the 128-word address range returns invalid data. The Secured Silicon Sector Indicator Bit, DQ7, (at Autoselect address 03h) is used to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory.

Please note the following general conditions:

- On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.
- Reads outside of sector SA0 return memory array data.
- Sector SA0 is remapped from memory array to Secured Silicon Sector array.
- Once the Secured Silicon Sector Entry Command is issued, the Secured Silicon Sector Exit command must be issued to exit Secured Silicon Sector Mode.
- The Secured Silicon Sector is not accessible when the device is executing an Embedded Program or Embedded Erase algorithm.
- The ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.

Factory Locked Secured Silicon Sector

The Factory Locked Secured Silicon Sector is always protected when shipped from the factory and has the Secured Silicon Sector Indicator Bit (DQ7) permanently set to a “1”. This prevents cloning of a factory locked part and ensures the security of the ESN and customer code once the product is shipped to the field.

These devices are available pre-programmed with one of the following:

- A random, 8 Word secure ESN only within the Secured Silicon Sector (at addresses 000000H - 000007H)
- Both a random, secure ESN and customer code through the Spansion programming service.

Customer Lockable Secured Silicon Sector

The Customer Lockable Secured Silicon Sector is always shipped unprotected (DQ7 set to “0”), allowing customers to utilize that sector in any manner they choose. If the security feature is not required, the Secured Silicon Sector can be treated as an additional Flash memory space.

Please note the following:

- Once the Secured Silicon Sector area is protected, the Secured Silicon Sector Indicator Bit is permanently set to “0.”
- The Secured Silicon Sector can be read any number of times, but can be programmed and locked only once. The Secured Silicon Sector lock must be used with caution as once locked, there is no procedure available for unlocking the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.
- The accelerated programming (ACC) and unlock bypass functions are not available when the Secured Silicon Sector is enabled.
- Once the Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence which return the device to the memory array at sector 0.

Secured Silicon Sector Entry/Exit Command Sequences

The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence.

See Command Definitions [Secured Silicon Sector Command Table, Appendix Table 39 (Pg 30) for address and data requirements for both command sequences.

The Secured Silicon Sector Entry Command allows the following commands to be executed

- Read customer and factory Secured Silicon areas
- Program the customer Secured Silicon Sector

After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by sector SA0 within the memory array. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device.

TABLE 1 – SECTOR & MEMORY ADDRESS MAP

Uniform Sector Size	Sector Count	Sector Range	Address Range (16-bit)	Notes
Sector Count	128	SA00	0000000h - 000FFFFh	Sector Starting Address
		:		
		SA127	07F0000 - 7FFFFF	Sector Ending Address

TABLE 2 – DEVICE OPERATIONS

Operation	CE#	OE#	WE#	RESET#	WP3/ACC	Addresses (Note 1)	DQ0 - DQ7	DQ8 - DQ15
Read	L	L	H	H	X	A_{IN}	D_{OUT}	D_{OUT}
Write (Program/Erase)	L	H	L	H	(Note 2)	A_{IN}	(Note 3)	(Note 3)
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 3)	(Note 3)
Standby	V_{CC} ± 0.3V	X	X	V_{CC} ± 0.3V	H	X	High-Z	High-Z
Output Disable	L	H	H	H	X	X	High-Z	High-Z
Reset	X	X	X	L	X	X	High-Z	High-Z

Legend

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{HH} = 11.5–12.5V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes

1. Addresses are AMax:A0 in word mode; AMax.
2. If WP# = V_{IL}, on the outermost sector remians protected. If WP# = V_{IH}, the outermost secotr is unprotected. WP# has an internal pull-up; when uconnected, WP# is a V_{IH}. All sectors are unprotected wen shipped from the factory (The Secured Silicon Sector can be factory protected depending on version ordered.)
3. D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm.

TABLE 3 – AUTOSELECT CODES, (HIGH VOLTAGE METHOD)

Description		CE#	OE#	WE#	Amax to A16	A14 to A10	A9	A8 to A7	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Device ID	Cycle 1	L	L	H	X	X	V_{ID}	X	L	L	L	H	22	7Eh
	Cycle 2									H	H	L	22	21h
	Cycle 3									H	H	H	22	01h
Sector Group Protection Verification		L	L	H	SA	X	V_{ID}	X	L	L	H	L	X	01h (unprotected), 00h (unprotected)
Secured Silicon Sector Indicator Bit (DQ7), WP# protects highest address sector		L	L	H	X	X	V_{ID}	X	L	L	H	H	X	99h (factory locked), 19h (not factory locked)
Secured Silicon Sector Indicator Bit (DQ7), WP# protects lowest address sector		L	L	H	X	X	V_{ID}	X	L	L	H	H	X	89h (factory locked), 09h (not facotry locked)

Legend

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care. V_{ID} = 11.5V to 12.5V

TABLE 4 – AUTOSELECT ADDRESSES IN SYSTEM

Uniform Sector Size	Sector Count	Read Data (word mode)
Manufacturer ID	(Base) + 00h	xx02h
Device ID, Word 1	(Base) + 01h	227Eh
Device ID, Word 2	(Base) + 0Eh	2221h
Device ID, Word 3	(Base) + 0Fh	2201h
Secure Device Verify	(Base) + 03h	XX19h = Note Factory Locked. XX99h = Factory locked
		XX09h = Note Factory Locked. XX89h = Factory locked
Sector Protect Verify	(SA) + 02h	xx01h = Locked. XX00h = Unlocked

TABLE 5 – AUTOSELECT ENTRY IN SYSTEM

Cycle	Operation	Word Address	Data
Unlock Cycle 1	Write	Base + 555h	0x00AAh
Unlock Cycle 2		Base + 2AAh	0x0055h
Auto select Command		Base + 555h	0x0090h

TABLE 6 – AUTOSELECT EXIT

Cycle	Operation	Word Address	Data
Unlock Cycle 1	Write	Base + XXXh	0x00F0h

Note
1. Any offset within the device works.
2. base = base address.

TABLE 7 – SINGLE WORD PROGRAM

(LLD Function = lld_ProgramCmd)

Cycle	Operation	Word Address	Data
Unlock Cycle 1	Write	Base + 555h	00AAh
Unlock Cycle 2		Base + 2AAh	0055h
Program Setup		Base + 555h	00A0h
Program		Word Address	Data

TABLE 8 – WRITE BUFFER PROGRAM

(LLD Functions Used = lld_WriteToBufferCmd, lld_ProgramBufferToFlashCmd)

Cycle	Description	Operation	Word Address	Data
1	Unlock	Write	Base + 555h	00AAh
2	Unlock		Base + 2AAh	0055h
3	Write Buffer Load Command		Sector Address	0025h
4	Write Word Count		Sector Address	Word Count (N-1)h
Number of words (N) loaded into the write buffer can be from 1 to 32 words.				
5 to 36	Load Buffer Word N	Write	Program Address, Word N	Word N
Last	Write Buffer to Flash		Sector Address	0029h

Notes
1. Base = Base Address.
2. Last = Last cycle of write buffer program operation; depending on number of words written, the total number of cycles may be from 6 to 37.
3. For maximum efficiency, it is recommended that the write buffer be loaded with the highest number of words (N words) possible.

TABLE 9 – SECTOR ERASE

(LLD Function = lld_SectorEraseCmd)

Cycle	Description	Operation	Word Address	Data
1	Unlock	Write	Base + 555h	00AAh
2	Unlock		Base + 2AAh	0055h
3	Setup Command		Base + 555h	0080h
4	Unlock		Base + 555h	00AAh
5	Unlock		Base + 2AAh	0055h
6	Sector Erase Command		Sector Address	0030h
Unlimited additional sectors may be selected for erase; command(s) must be written within 50µs				

Notes
1. Base = Base Address.
2. Last = Last cycle of write buffer program operation; depending on number of words written, the total number of cycles may be from 6 to 37.
3. For maximum efficiency, it is recommended that the write buffer be loaded with the highest number of words (N words) possible.

TABLE 10 – SECTOR ERASE

(LLD Function = lld_SectorEraseCmd)

Cycle	Description	Operation	Word Address	Data
1	Unlock	Write	Base + 555h	00AAh
2	Unlock		Base + 2AAh	0055h
3	Setup Command		Base + 555h	0080h
4	Unlock		Base + 555h	00AAh
5	Unlock		Base + 2AAh	0055h
6	Chip Erase Command		Base + 555h	0010h

TABLE 11 – ERASE SUSPEND

(LLD Function = lld_EraseSuspendCmd)

Cycle	Operation	Word Address	Data
1	Write	Base + XXXh	00B0h

TABLE 12 – ERASE RESUME

(LLD Function = lld_EraseSuspendCmd)

Cycle	Operation	Word Address	Data
1	Write	Sector Address	0030h

TABLE 13 – PROGRAM SUSPEND

(LLD Function = lld_ProgramSuspendCmd)

Cycle	Operation	Word Address	Data
1	Write	Base + XXXh	00B0h

TABLE 14 – PROGRAM RESUME

(LLD Function = lld_ProgramSuspendCmd)

Cycle	Operation	Word Address	Data
1	Write	Base + XXXh	0030h

TABLE 15 – UNLOCK BYPASS ENTRY

(LLD Function = lld_UnlockBypassEntryCmd)

Cycle	Description	Word Address	Data
1	Unlock	Base + 555h	00AAh
2	Unlock	Base + 2AAh	0055h
3	Entry Command	Base + 555h	0020h

TABLE 16 – UNLOCK BYPASS PROGRAM

(LLD Function = lld_UnlockBypassProgramCmd)

Cycle	Description	Word Address	Data
1	Program Setup Command	Base + xxxh	00AAh
2	Program Command	Program Address	0055h

TABLE 17 – UNLOCK BYPASS PROGRAM

(LLD Function = lld_UnlockBypassProgramCmd)

Cycle	Description	Word Address	Data
1	Reset Cycle 1	Base + xxxh	0090h
2	Reset Cycle 2	Base + xxxh	0000h

TABLE 18 – WRITE OPERATION STATUS

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	DQ1	RY/BY#
Standard Mode		Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0	0
		Embedded Erase Algorithm	0	Toggle	0	1	Toggle	N/A	0
Program Suspend Mode	Program Suspend Read	Program-Suspended Sector	Invalid (not allowed)						1
		Non-Suspend Sector	Data						1
Erase Suspend Mode	Erase-Suspend Read	Erase-Suspended Sector	1	No toggle	0	N/A	Toggle	N/A	1
		Non-Erase Suspended Sector	Data						1
	Erase-Suspend-Program (Embedded Program)		DQ7#	Toggle	0	N/A	N/A	N/A	0
Write-to-Buffer	Busy (Note 3)		DQ7#	Toggle	0	N/A	N/A	0	0
	Abort (Note 4)		DQ7#	Toggle	0	N/A	N/A	1	0

Notes
1. DQ5 switches to 1 when an Embedded Program, Embedded Erase, or Write-to-Buffer operation has exceeded the maximum timing limits. Refer toDQ5: Exceeded Timing Limits on page 39 for more information.
2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
3. The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.
4. DQ1 switches to 1 when the device has aborted the write-to-buffer operation

TABLE 19 – SOFTWARE FUNCTIONS RESET

(LLD Function = lld_ResetCmd)

Cycle	Operation	Word Address	Data
Reset Command	Write	Base + xxxh	00F0h

TABLE 20 LOCK REGISTER

DQ15-3	DQ2	DQ1	DQ0
Don't Care	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	Secured Silicon Sector Protection Bit

TABLE 21 – SECTOR PROTECTION SCHEMES: DYB, PPB AND PPB LOCK BIT COMBINATIONS

Uniques Device PPB Lock Bit 0 = locked 1 = unlock		Sector PPB 0 = locked 1 = unlock	Sector DYB 0 = locked 1 = unlock	Sector Protection Status
Any Sector	0	0	x	Protected through PPB
Any Sector	0	0	x	Protected through PPB
Any Sector	0	1	1	Unportected
Any Sector	0	1	0	Protected through PPB
Any Sector	1	0	x	Protected through PPB
Any Sector	1	0	x	Protected through PPB
Any Sector	1	1	0	Protected through PPB
Any Sector	1	1	1	Unportected

Table 21 contains all possible combinations of the DYB, PPB, and PPB Lock Bit relating to the status of the sector. In summary, if the PPB Lock Bit is locked (set to “0”), no changes to the PPBs are allowed. The PPB Lock Bit can only be unlocked (reset to “1”) through a hardware reset or power cycle.

TABLE 22 – LOCK REGISTER

Secured Silicon Sector Address Range	Customer Lockable	ESN Factory Locked	ExpressFlash Factory Locked
000000h-000007h	Determined by customer	ESN	ESN or determinded by customer
000008h-000007Fh		Unavailable	Determinined by customer

TABLE 23 – SECURED SILICON SECTOR ENTRY

(LLD Function = lld_SecSiSectorEntryCmd)

Cycle	Operation	Word Address	Data
Unlock Cycle 1	Write	Base + 555h	00AAh
Unlock Cycle 2		Base + 2AAh	0055h
Entry Cycle		Base + 555h	0088h

Note:
Base = Base Address.

TABLE 24 – SECURED SILICON SECTOR PROGRAM

(LLD Function = lld_ProgramCmd)

Cycle	Operation	Word Address	Data
Unlock Cycle 1	Write	Base + 555h	00AAh
Unlock Cycle 2		Base + 2AAh	0055h
Program Setup		Base + 555h	0088h
Program		Word Address	Data Word

Note:
Base = Base Address.

TABLE 25 – SECURED SILICON SECTOR EXIT

(LLD Function = lld_SecSiSectorExitCmd)

Cycle	Operation	Word Address	Data
Unlock Cycle 1	Write	Base + 555h	00AAh
Unlock Cycle 2		Base + 2AAh	0055h
Exit Cycle 3		Base + 555h	0088h
Exit Cycle 4		Base + 000h	0000h

Note:
Base = Base Address.

TABLE 26 – ABSOLUTE MAXIMUM RATINGS

Description		Rating
Storage Temperature		-55ºC to +125ºC
Ambient Temperature with Power Applied		
Voltage with Respect to Ground	All Inputs and I/Os except as noted below (Note 1)	-0.5V to VCC + 0.5V
	V_{CC} (Note 1)	-0.5V to +4.0 V
	V_{IO}	-0.5V to +4.0 V
	A9 and ACC (Note 2)	0.5V to +12.5V

Notes

1. Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may undershoot VSS to –2.0 V for periods of up to 20 ns. See Figure 11. Maximum DC voltage on input or I/Os is V_{CC} + 0.5 V. During voltage transitions inputs or I/Os may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 12.
2. Minimum DC input voltage on pins A9 and ACC is -0.5V. During voltage transitions, A9 and ACC may overshoot VSS to –2.0 V for periods of up to 20 ns. See Figure 11. Maximum DC voltage on pins A9 and ACC is +12.5 V, which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
4. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 27 – CAPACITANCE

T_A = +25°C, f = 1.0MHz

Parameter	Symbol	Max	Unit
WE# capacitance	C_{WE}	13	pF
CS# capacitance	C_{CS}	25	pF
Data I/O capacitance	$C_{I/O}$	15	pF
Address input capacitance	C_{AD}	30	pF
RY/BY#	C_{RB}	40	pF
OE# capacitance	C_{OE}	35	pF

This parameter is guaranteed by design but not tested.

TABLE 28 – RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
I/O Supply Voltage	V_{IO}	3.0	3.6	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

Note: For all AC and DC specifications: $V_{IO} = V_{CC}$

TABLE 29 – DATA RETENTION

Parameter	Test Conditions	Min	Unit
Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

TABLE 30 – DC CHARACTERISTICS

Parameter Symbol	Parameter Description (Notes)	Test Conditions		Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC} $V_{CC} = V_{CC\ max}$	WP/ACC (3)		20	µA
			Others		8	
I_{LIT}	A9 Input Load Current (3)	$V_{CC} = V_{CC\ max}$; 12.5V			140	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$			4	µA
I_{CC1}	V_{CC} active Read Current (1)	CE# =V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$, f = 5MHz			440	mA
I_{IO2}	V_{IO} Non-active Output (3)	CE# =V_{IL}, OE# = V_{IH}			40	mA
I_{CC2}	V_{CC} Intra-Page Read Current (1)	CE# =V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$, f = 10MHz			40	mA
I_{CC3}	V_{CC} Active Erase/Program CUrrent (2, 3)	CE# =V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$			360	mA
I_{CC4}	V_{CC} Standby Current	CE#, RESET# =V_{CC} ±0.3V, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$ $V_{IL} = V_{SS}$ + 0.3V/-0.1V			20	µA
I_{CC5}	V_{CC} Reset Current	$V_{CC} = V_{CC\ max}$; RESET# = V_{SS} ±0.3V			2	mA
I_{CC6}	Automatic Sleep Mode (3, 4)	$V_{CC} = V_{CC\ max}$, $V_{IH} = V_{CC}$ ±0.3V, WP#/ACC = V_{IH}			20	µA
I_{ACC}	ACC Accelerated Program Current (3)	CE# = V_{IL}, OE# = V_{IH} $V_{CC} = V_{CC\ max}$, WP#/ACC = V_{HH}	WP#/ACC pin		80	mA
			V_{CC} pin		320	
V_{IL}	Input Low Voltage (5)			-0.1	0.3 x V_{IO}	V
V_{IH}	Input High Voltage (5)			0.7 x V_{IO}	V_{IO} + 0.3	V
V_{HH}	Voltage for Program Acceleration (3)	V_{CC} = 2.7 - 3.6V		11.5	12.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unportect (3)	V_{CC} = 2.7 - 3.6V		11.5	12.5	V
V_{OL}	Output Low Voltage (5)	I_{OL} = 100µA			0.15 x V_{IO}	V
V_{OH}	Output High Voltage (5)	I_{OH} = 100µA		0.85 x V_{IO}		V
V_{LKO}	Low V_{CC} Lock-Out Voltage (3)			2.3	2.5	V

Notes
1. The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.
2. I_{CC} active while Embedded Erase or Embedded Program or Write Buffer Programming is in progress.
3. Not 100% tested.
4. Automatic sleep mode enables the lower power mode when addresses remain stable tor t_{ACC} + 30 ns.
5. V_{IO} = 1.65–3.6 V
6. V_{CC} = 3 V and V_{IO} = 3V or 1.8V. When V_{IO} is at 1.8V, I/O pins cannot operate at 3V.

TABLE 31 – AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} - 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
VZ is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16 mA.
Tester Impedance Z0 = 50Ω.
VZ is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to similate a typical resistive load circuit.
ATE tester Includes jig capacitance.

FIGURE 4 – TEST SETUP

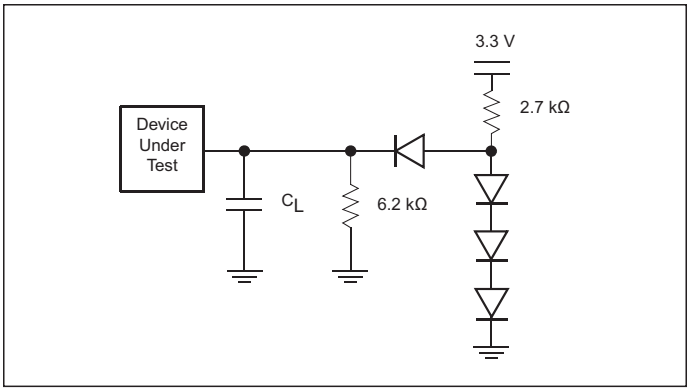


TABLE 32 – TEST SPECIFICATIONS

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, CL (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–V_{IO}	V
Input timing measurement reference levels (See Note)	0.5V_{IO}	V
Output timing measurement reference levels	0.5V_{IO}	V

Note: If V_{IO} < V_{CC}, the reference level is 0.5 V_{IO}.

TABLE 33 – AC CHARACTERISTICS – READ-ONLY OPERATIONS

V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ +125°C

Parameter		Symbol		-110 Min	-110 Max	-120 Min	-120 Max	Unit
Read Cycle Time		t_{AVAV}	t_{RC}	110		120		ns
Address Access Time		t_{AVQV}	t_{ACC}		110		120	ns
Chip Select Access Time		t_{ELQV}	t_{CE}		110		120	ns
Page Access Time			t_{PACC}		25		25	ns
Output Enable to Output Valid (1)		t_{GLQV}	t_{OE}		25		25	ns
Chip Select High to Output High Z		t_{EHQZ}	t_{DF}		20		20	ns
Output Enable High to Output High Z		t_{GHQZ}	t_{DF}		20		20	ns
Output Hold from Addresses, CS# or OE# Change, Whichever occurs first		t_{AXQX}	t_{OH}	0		0		ns
Output Enable Hold Time	Read		t_{OEH}	0		0		ns
	Toggle and Data# Polling			10		10		ns
Chip Enable Hold Time			t_{CEH}	35		35		ns

Note: 1. t_{OE} for data polling Zs 45ns when V_{IO} = 1.65 to 2.7V and 35ns when V_{IO} = 2.7 to 3V.

TABLE 34 – AC CHARACTERISTICS – HARDWARE RESET (1)

Parameter	Symbol	Min	Max	Unit
RESET# Pin Low (During Embedded Algorithms) to Read Mode	t_{ready}	35		µs
RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode	t_{ready}	35		µs
RESET# Pulse Width	t_{RP}	35		µs
RESET# High Time Before Read	t_{RH}	200		ns
RESET# Low to Standby Mode	t_{RPD}	10		µs
RY/BY# Recovery Time	t_{RB}	0		ns

TABLE 35 – POWER-UP SEQUENCE TIMINGS

Parameter	Symbol	Min	Max	Unit
Reset Low Time from rising edge of V_{CC} (or last Reset pulse) to rising edge of RESET#	tV_{CS}	35		µs
Reset Low Time from rising edge of V_{IO} (or last Reset pulse) to rising edge of RESET#	tV_{IOS}	35		µs
Reset High Time before Read	t_{RH}	200		µs

Notes
1. $V_{IO} < V_{CC}$ + 200 mV.
2. V_{IO} and V_{CC} ramp must be synchronized during power up.
3. If RESET# is not stable for tV_{CS} or tV_{IOS}:
   The device does not permit any read and write operations.
   A valid read operation returns FFh.
   A hardware reset is required.
4. V_{CC} maximum power-up current (RST=V_{IL}) is 20 mA.

TABLE 36 – AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – WE# CONTROLLED

V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-110 Min	-110 Max	-120 Min	-120 Max	Unit
Write Cycle Time	t_AV_AV	t_{WC}	110		120		ns
Chip Select Setup Time (3)	t_{ELWL}	t_{CS}	0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	35		35		ns
Address Setup Time	t_AV_{WL}	t_{AS}	0		0		ns
Data Setup Time	t_DV_{WH}	t_{DS}	30		30		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		45		ns
Write Enable Pulse Width High (3)	t_{WHWL}	t_{WPH}	30		30		ns
Duration of Byte Programming Operation	t_{WHWH1}			480		480	µs
Sector Erase (2)	t_{WHWH2}			5		5	sec
Read Recovery Time before Write (3)	t_{GHWL}		0		0		ns
V_{CC} Setup Time (3)	tV_{CS}		35		35		µs
Chip Programming Time (4)				200		200	sec
Address Setup Time to OE# low during toggle bit polling		t_{ASO}	15		15		ns

Notes:
1. Typical value for t_{WHWH1} is 6µs.
2. Typical value for t_{WHWH2} is 0.5 sec.
3. Guaranteed by design, but not tested.
4. Typical value is 50 sec. The typical chip program time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.

TABLE 37 – AC CHARACTERISTICS – ALTERNATE CS# CONTROLLED ERASE AND PROGRAM OPERATIONS

Parameter		Description		Speed Options		Unit
JEDEC	Std			110	120	
t_{AVAV}	t_{WS}	Write Cycle Time	Min	110	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	30	30	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	0	ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0	0	ns
t_{ELEH}	t_{CP}	CS# Pulse Width	Min	35	35	ns
t_{EHEL}	t_{CPH}	CS# Pulse Width High (1)	Min	30	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Typ	480	480	µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation	Typ	13.5	13.5	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Typ	0.5	0.5	sec

Note:
1. Not tested.

TABLE 38 – ERASE AND PROGRAMMING PERFORMANCE

V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ +125°C

Parameter	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	0.5	3.5	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	64	256	sec	
Total Write Buffer Time (Note 3)	480		µs	Excludes system level overhead (Note 5)
Total Accelerated Write Buffer Programming Time (Note 3)	432		µs	
Ship Program Time	123		sec	

Notes
1. Typical program and erase times assume the following conditions: 25ºC, 3.6V V_{CC}, 10,000 cycles, checker board pattern.
2. Under corst case conditions of -40ºC, V_{CC} = 3.0V, 100,000 cycle.
3. Effective write buffer specification is based upon 32-word write buffer operation.
4. In the pre-programming step of the embedded erase algorithm, all bits are programmed to 00H before erasure.
5. System0level overhead is the time required to execute the two-or four-bus-cycle sequence for the program command. See table 38 and 39.

TABLE 39 – MEMORY ARRAY COMMAND DEFINITIONS

Command		Cycles	Bus Cycles (Note 1-5)											
			First		Second		Third		Fouth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (6)		1	RA	RD										
Reset (7)		1	XXX	F0										
AutoSelect (8, 9)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
	Device ID (8)	4	555	AA	2AA	55	555	90	X01	227E	X0E	(8)	X0F	(8)
	Sector Protect Verify (10)	4	555	AA	2AA	55	555	90	[SA]X02	(10)				
	Secure Device Verify (11)	4	555	AA	2AA	55	555	90	X03	(11)				
CFI Query (12)		1	55	98										
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer		3	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD
Program Buffer to Flash (Confirm)		1	SA	29										
Write-to-Buffer-Abort Reset		3	555	AA	2AA	55	555	F0						
Unlock Bypass	Enter	3	555	AA	2AA	55	555	20						
	Program (14)	2	XXX	A0	PA	PD								
	Sector Erase (14)	2	XXX	80	SA	30								
	Chip Erase (14)	2	XXX	80	XXX	10								
	Reset (15)	2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend/Program Suspend (16)		1	XXX	B0										
Erase Resume/Program Resume (17)		1	XXX	30										
Secured Silicon Sector Entry		3	555	AA	2AA	55	555	88						
Secured SIlicon Sector Exit (18)		4	555	AA	2AA	55	555	90	XX	00				

LEGEND

X = Don't care

RA = Address of the memory to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits Amax–A16 uniquely select any sector.

WBL = Write Buffer Location. The address must be within the same write buffer page as PA.

WC = Word Count is the number of write buffer locations to load minus 1.

NOTES

1. See Table 2 for description of bus operations.
2. All values are in hexadecimal.
3. All bus cycles are write cycles unless otherwise noted.
4. Data bits DQ15-DQ8 are don't cares for unlock and command cycles.
5. Address bits AMAX:A16 are don't cares for unlock and command cycles, unless SA or PA required. (AMAX is the Highest Address pin.).
6. No unlock or command cycles required when reading array data.
7. The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).
8. See Table 3 for device ID values and definitions.
9. The fourth, fifth, and sixth cycles of the autoselect command sequence are read cycles.
10. The data is 00h for an unprotected sector and 01h for a protected sector. See Autoselect for more information. This is same as PPB Status Read except that the protect and unprotect statuses are inverted here.
11. The data value for DQ7 is "1" for a serialized, protected Secured Silicon Sector region and "0" for an unserialized, unprotected region. See data and definitions.
12. Command is valid when device is ready to read array data or when device is in autoselect mode.
13. Command sequence returns device to reading array after being placed in a Write-to-Buffer-Abort state. Full command sequence is required if resetting out of abort while in Unlock Bypass mode.
14. The Unlock-Bypass command is required prior to the Unlock-Bypass- Program command.
15. The Unlock-Bypass-Reset command is required to return to reading array data when the device is in the unlock bypass mode.
16. The system can read and program/program suspend in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
17. The Erase Resume/Program Resume command is valid only during the Erase Suspend/ Program Suspend modes.
18. The Exit command returns the device to reading the array.

TABLE 40 – SECTOR PROTECTION COMMAND DEFINITIONS

Command		Cycles	Bus Cycles (Note 1-5)											
			First		Second		Third		Fouth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register	Command Set Entry	3	555	AA	2AA	55	555							
	Program (6)	2	XXX	A0	XXX	DATA								
	Read (6)	1	00	RD										
	Command Set Exit (7, 8)	2	XXX	90	XXX	00								
Password	Command Set Entry	3	555	AA	2AA	55	555							
	Password Program (9)	2	XXX	A0	PWAx	PWDx								
	Password Read (10)	4	00	PWD0	01	PWD 1	02	PWD 2	03	PWD 3				
	Password Unlock (10)	7	00	25	00	03	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3
			00	29										
	Command Set Exit (7, 8)	2	XXX	90	XXX	00								
Global Non-Volatile	PPB Command Set Entry	3	555	AA	2AA	55	555							
	PPB Program (11, 12)	2	XXX	A0	SA	00								
	All PPB Erase (13)	2	XXX	80	00	30								
	PPB Status Read (12)	1	SA	RD (0)										
	PPB Command Set Exit (7, 8)	2	XXX	90	XXX	00								
Global Volatile Freeze	PPB Lock Command Set Entry	3	555	AA	2AA	55	555							
	PPB Lock Set (12)	2	XXX	A0	XXX	00								
	PPB Lock Command Set Exit (7, 8)	1	XXX	RD (0)										
	PPB Lock Command Set Exit (7, 8)	2	XXX	90	XXX	00								
Volatile	DYB Command Set Entry	3	555	AA	2AA	55	555							
	DYB Set (11, 12)	2	XXX	A0	SA	00								
	DYB Clear (12)	2	XXX	A0	SA	01								
	DYB Status Read (12)	1	SA	RD (0)										
	DYB Command Set Exit (7, 8)	2	XXX	90	XXX	00								

LEGEND
X = Don't care
RD(0) = Read data.
SA = Sector Address. Address bits Amax–A16 uniquely select any sector.
PWD = Password
PWDx = Password word0, word1, word2, and word3.
Data = Lock Register Contents: PD(0) = Secured Silicon Sector Protection Bit,
PD(1) = Persistent Protection Mode Lock Bit, PD(2) = Password Protection Mode Lock Bit.

NOTES
1. See Table 2 for description of bus operations.
2. All values are in hexadecimal.
3. All bus cycles are write cycles unless otherwise noted.
4. Data bits DQ15-DQ8 are don't cares for unlock and command cycles.
5. Address bits AMAX:A16 are don't cares for unlock and command cycles, unless SA or PA required. (AMAX is the Highest Address pin.)
6. All Lock Register bits are one-time programmable. Program state = "0" and the erase state = "1." The Persistent Protection Mode Lock Bit and the Password Protection Mode Lock Bit cannot be programmed at the same time or the Lock Register Bits Program operation aborts and returns the device to read mode. Lock Register bits that are reserved for future use default to "1's." The Lock Register is shipped out as "FFFF's" before Lock Register Bit program execution.
7. The Exit command returns the device to reading the array.
8. If any Command Set Entry command was written, an Exit command must be issued to reset the device into read mode.
9. For PWDx, only one portion of the password can be programmed per each "A0" command.
10. Note that the password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.
11. If ACC = V_{HH}, sector protection matches when ACC = V_{IH}.
12. Protected State = "00h," Unprotected State = "01h."
13. The All PPB Erase command embeds programming of all PPB bits before erasure.

FIGURE 5 – SINGLE WORD PROGRAM

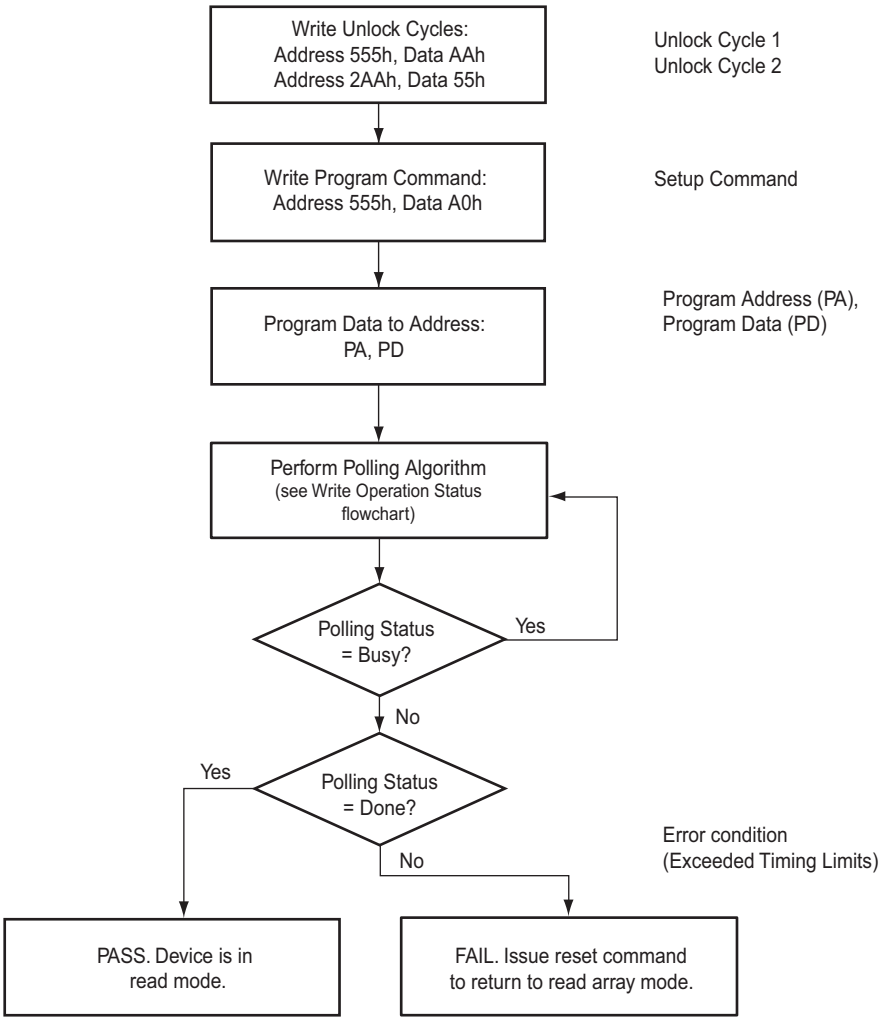


FIGURE 6 – WRITE BUFFER PROGRAMMING OPERATION

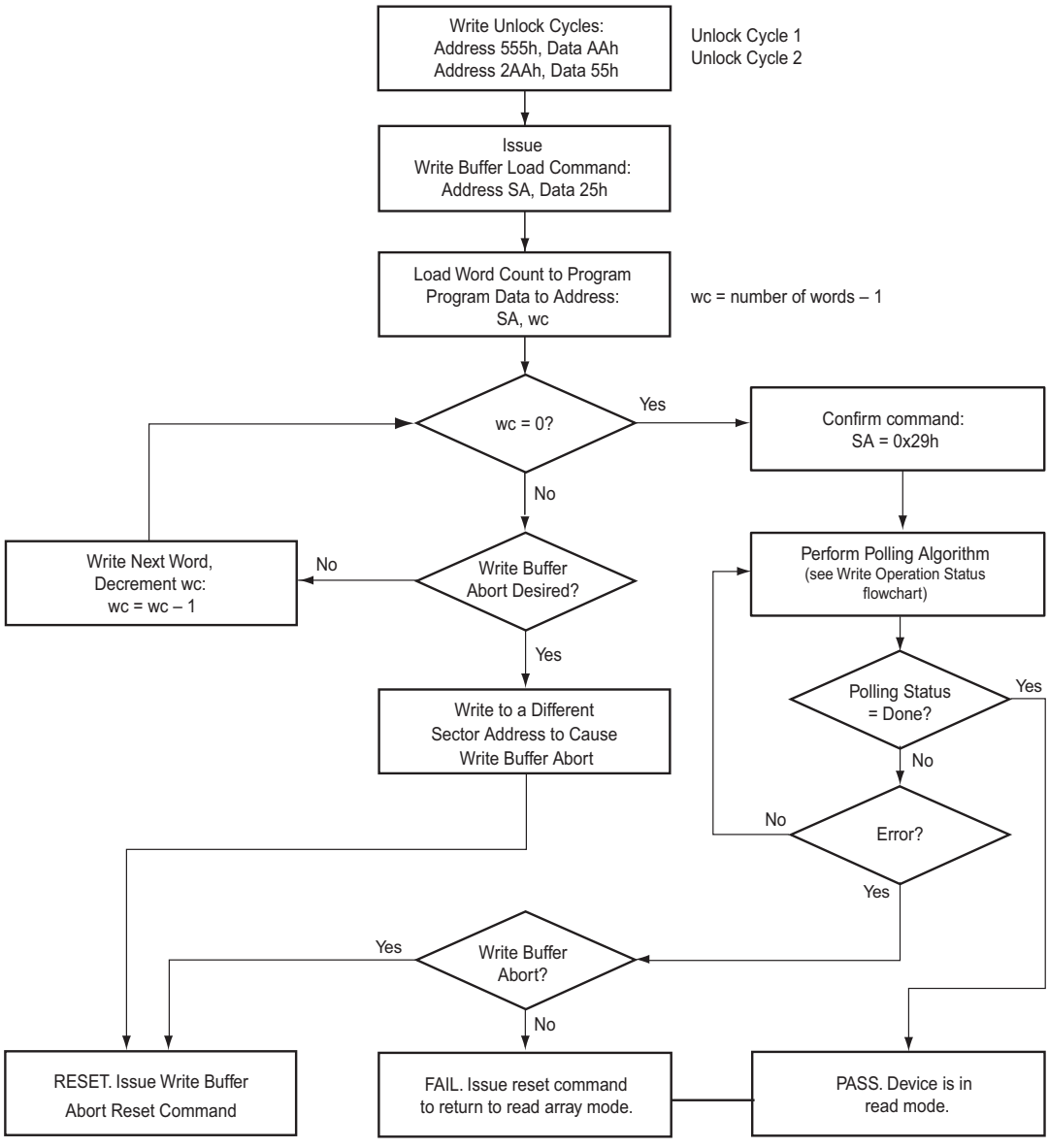
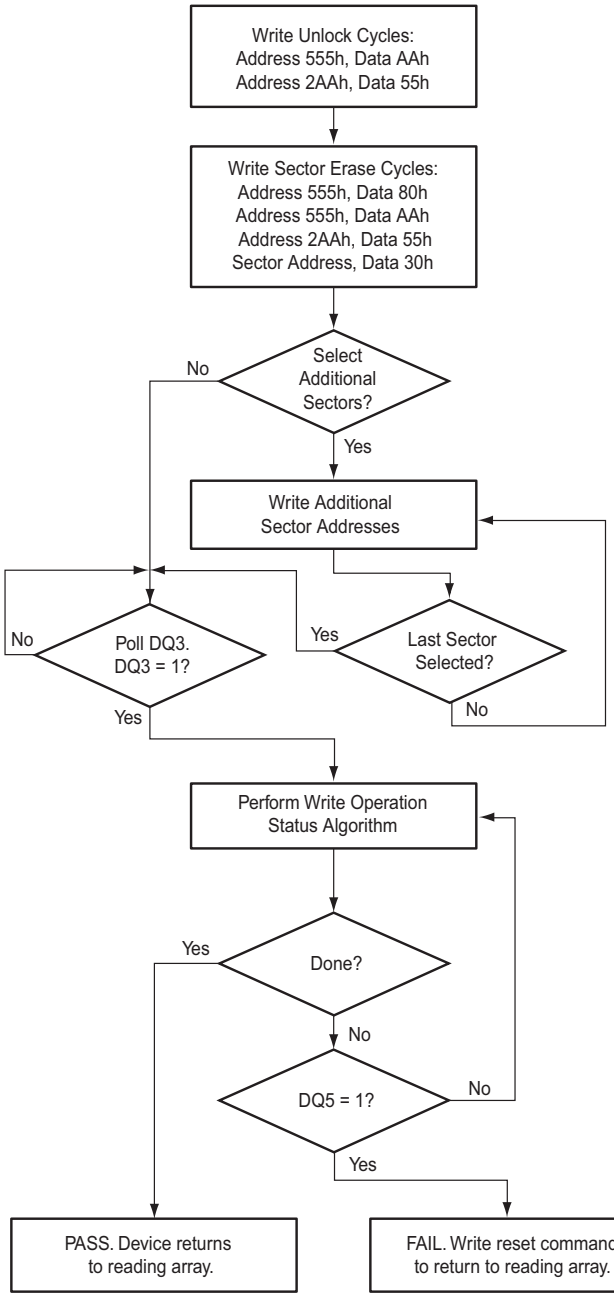


FIGURE 7 – SECTOR ERASE OPERATION



Unlock Cycle 1
Unlock Cycle 2

Command Cycle 1
Command Cycle 2
Command Cycle 3
Specify first sector for erasure

- Each additional cycle must be written within t_{SEA} timeout
- The host system may monitor DQ3 or wait t_{SEA} to ensure acceptance of erase commands
- No limit on number of sectors
- Commands other than Erase Suspend or selecting additional sectors for erasure during timeout reset device to reading array data

Status may be obtained by reading DQ7, DQ6 and/or DQ2.

Error condition (Exceeded Timing Limits)

Notes
1. See table 12.1 on page 69 for earse command sequence.
2. See DQ3: Sector Erase Timeout State Indicator on page 39 for information on the sector erase timeout.

FIGURE 8 – WRITE OPERATION STATUS FLOWCHART

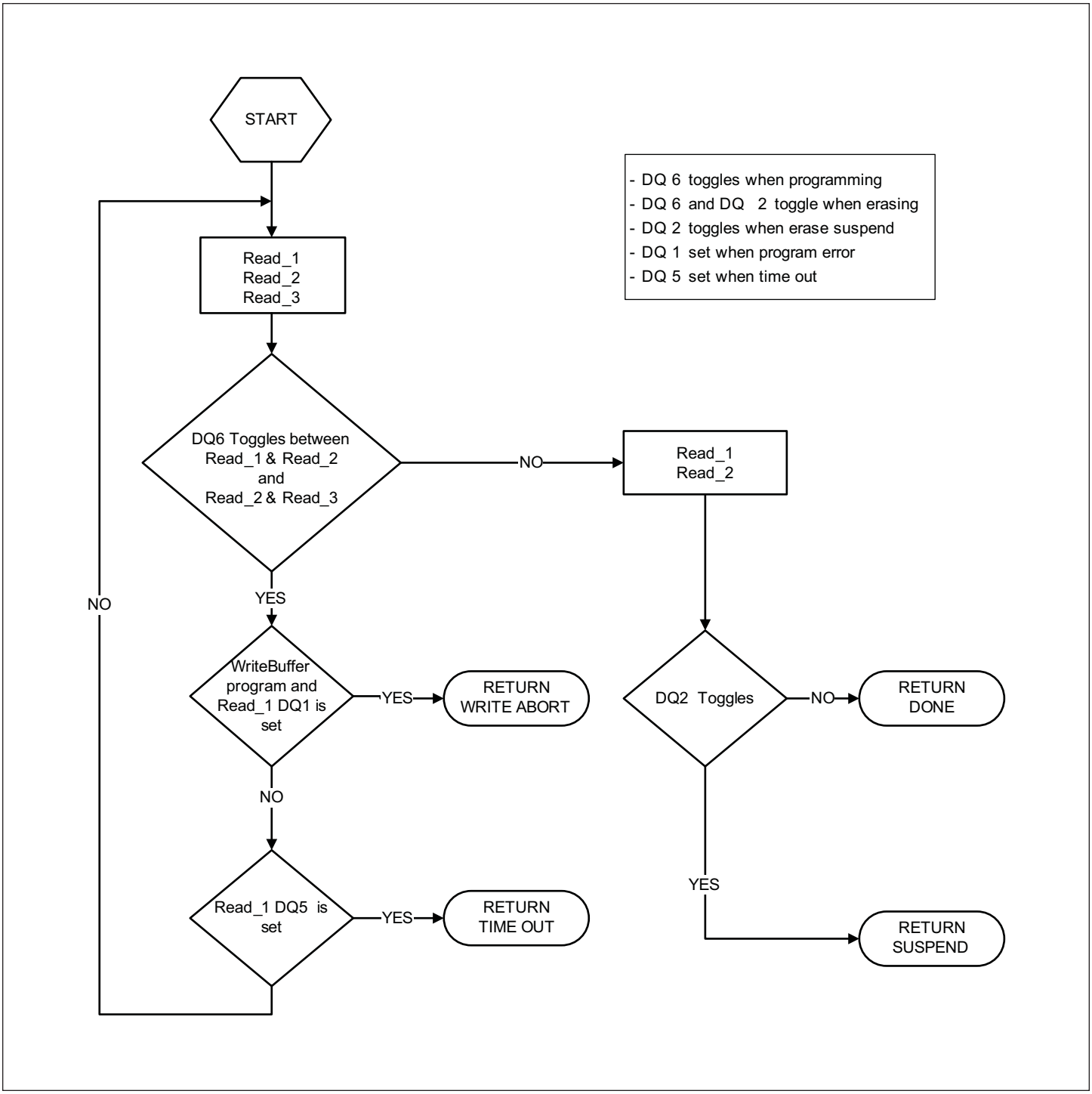


FIGURE 9 – ADVANCED SECTOR PROTECTION/UNPROTECTION

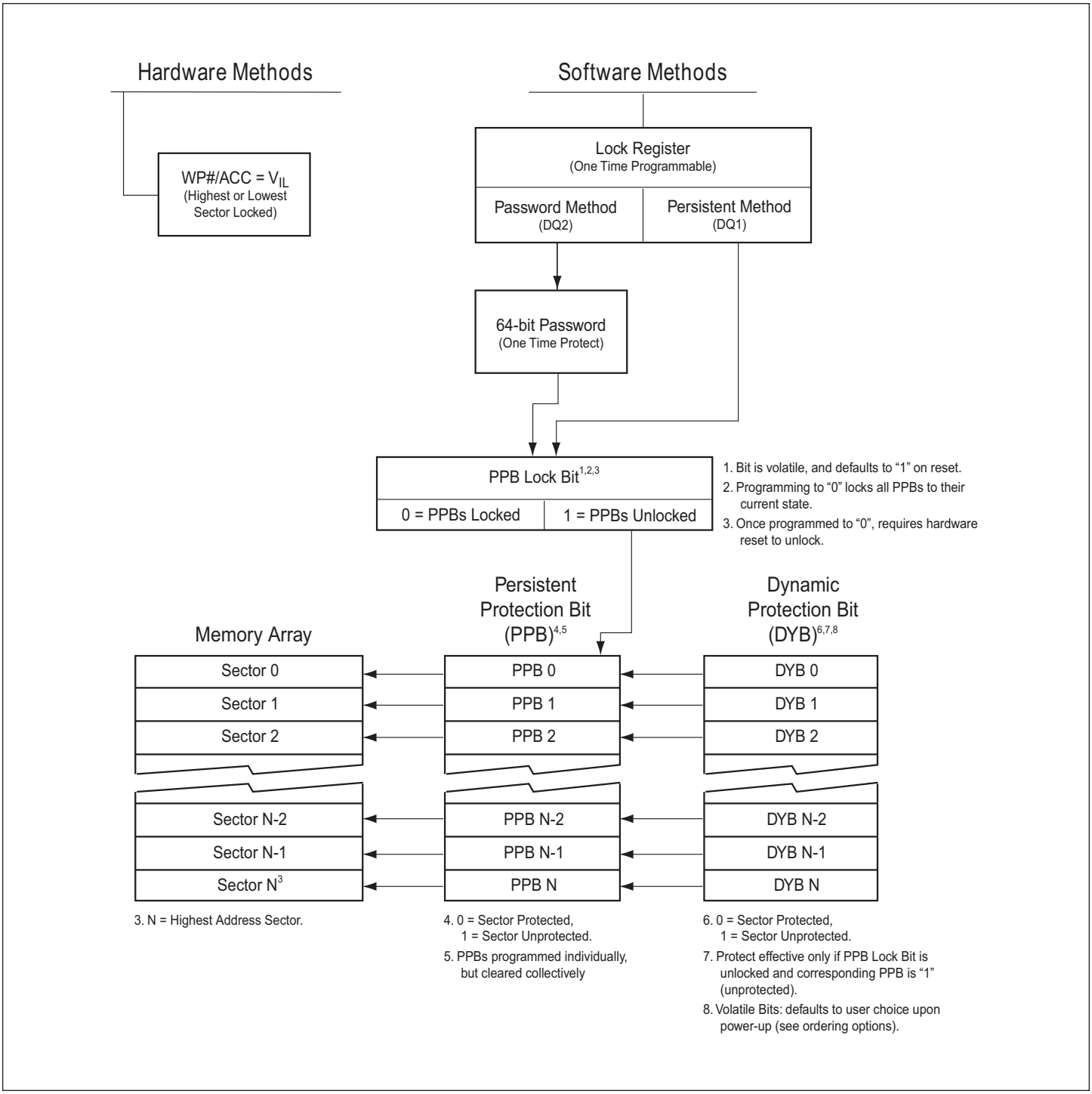


FIGURE 10 – PPB PROGRAM ALGORITHM

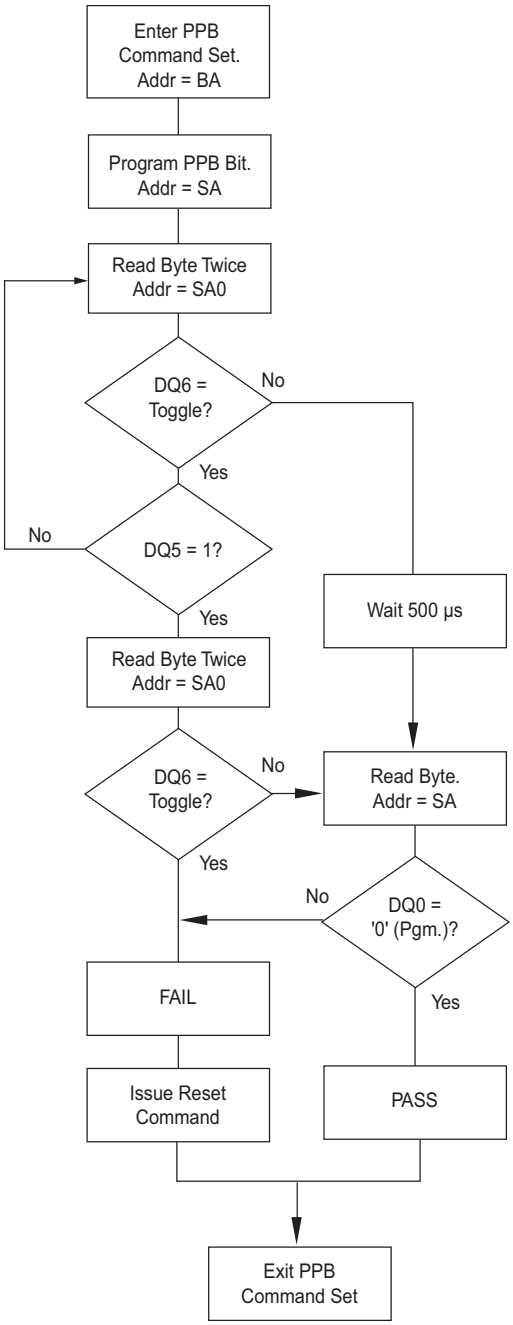


FIGURE 11 – LOCK REGISTER PROGRAM ALGORITHM

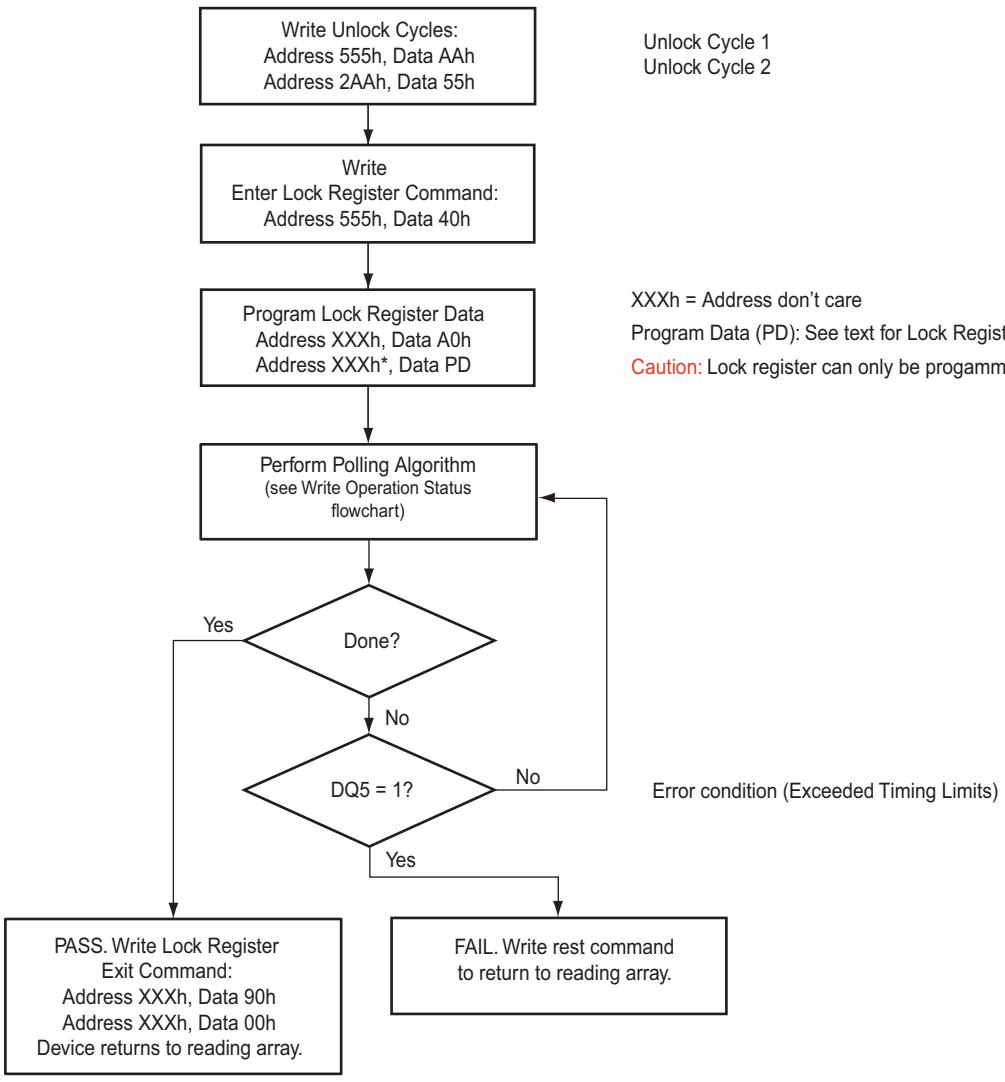


FIGURE 12 – MAXIMUM NEGATIVE OVERSHOOT WAVERFORM

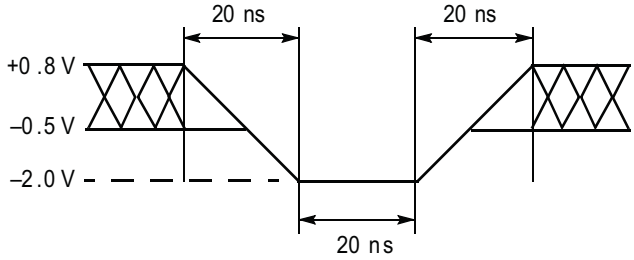


FIGURE 13 – MAXIMUM POSITIVE OVERSHOOT WAVERFORM

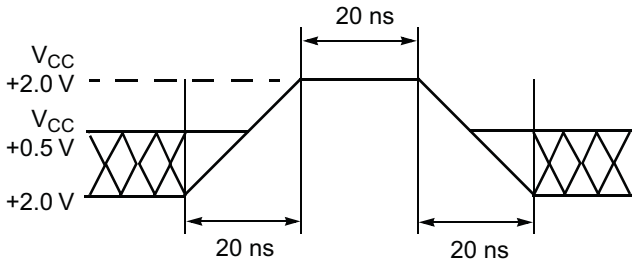


FIGURE 14 – AC TEST CIRCUIT

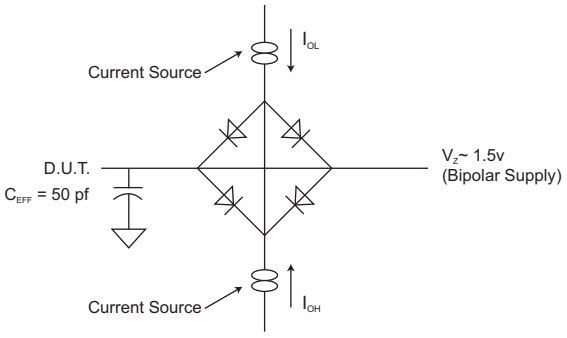


FIGURE 15 – AC WAVEFORMS FOR READ OPERATIONS

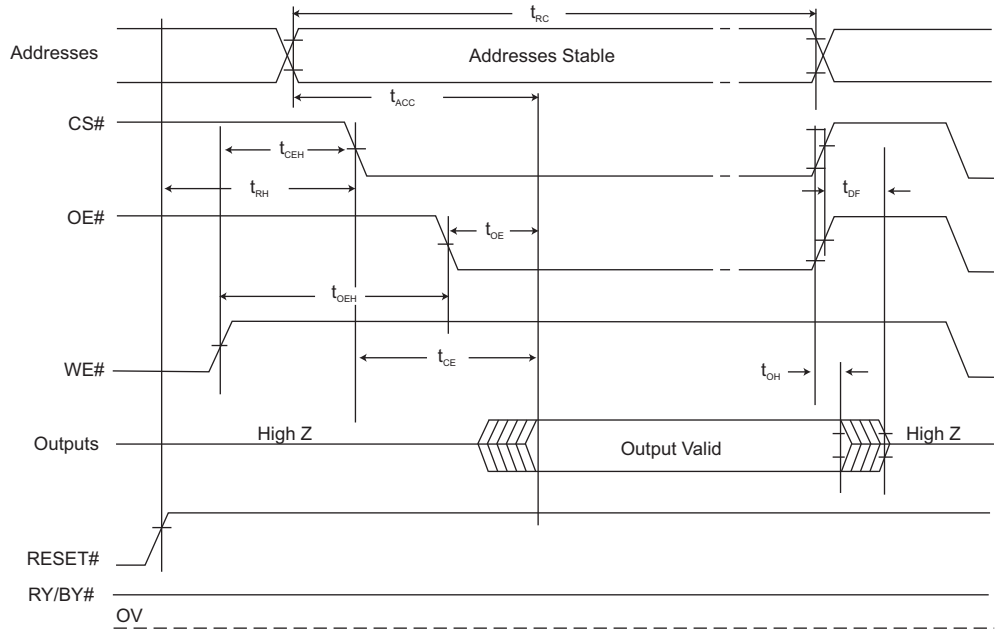


FIGURE 16 – PAGE READ OPERATION TIMINGS

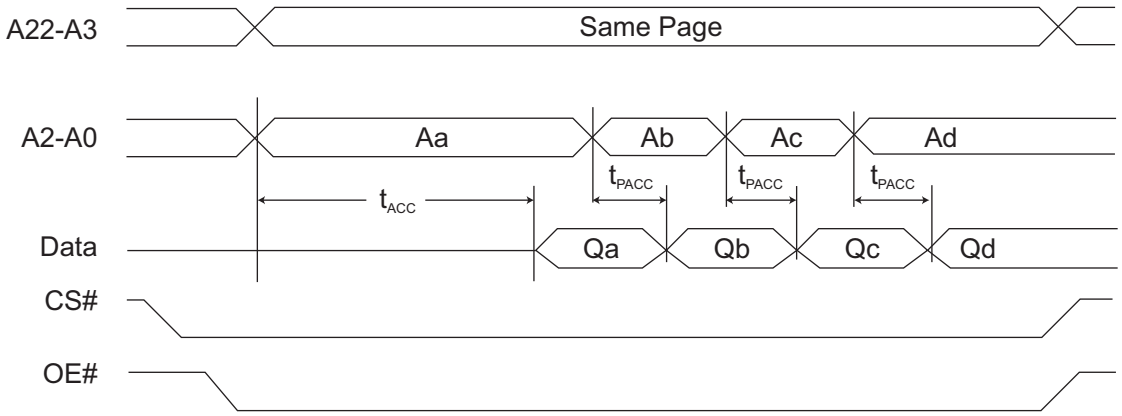


FIGURE 17 – RESET TIMINGS NOT DURING EMBEDDED ALGORITHMS

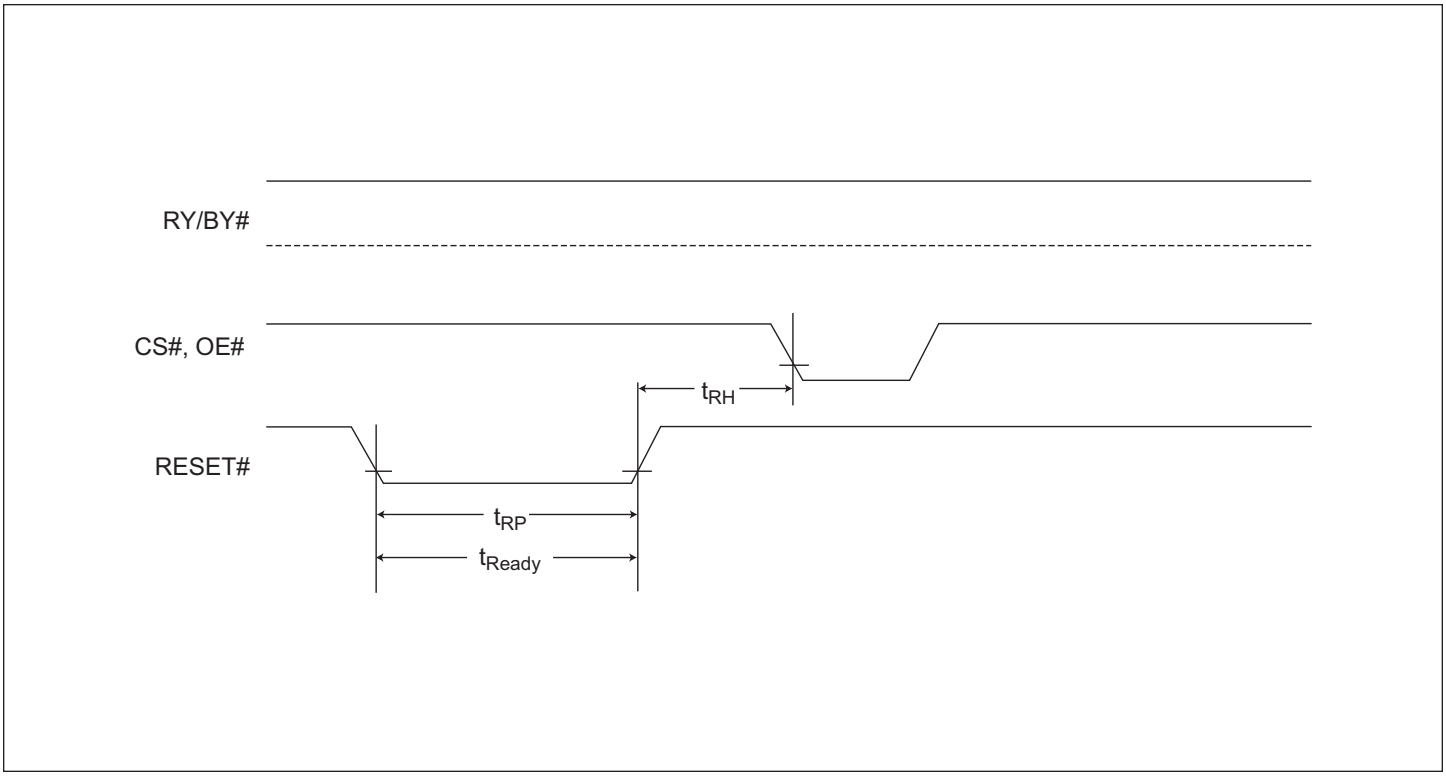


FIGURE 18 – RESET TIMINGS DURING EMBEDDED ALGORITHMS

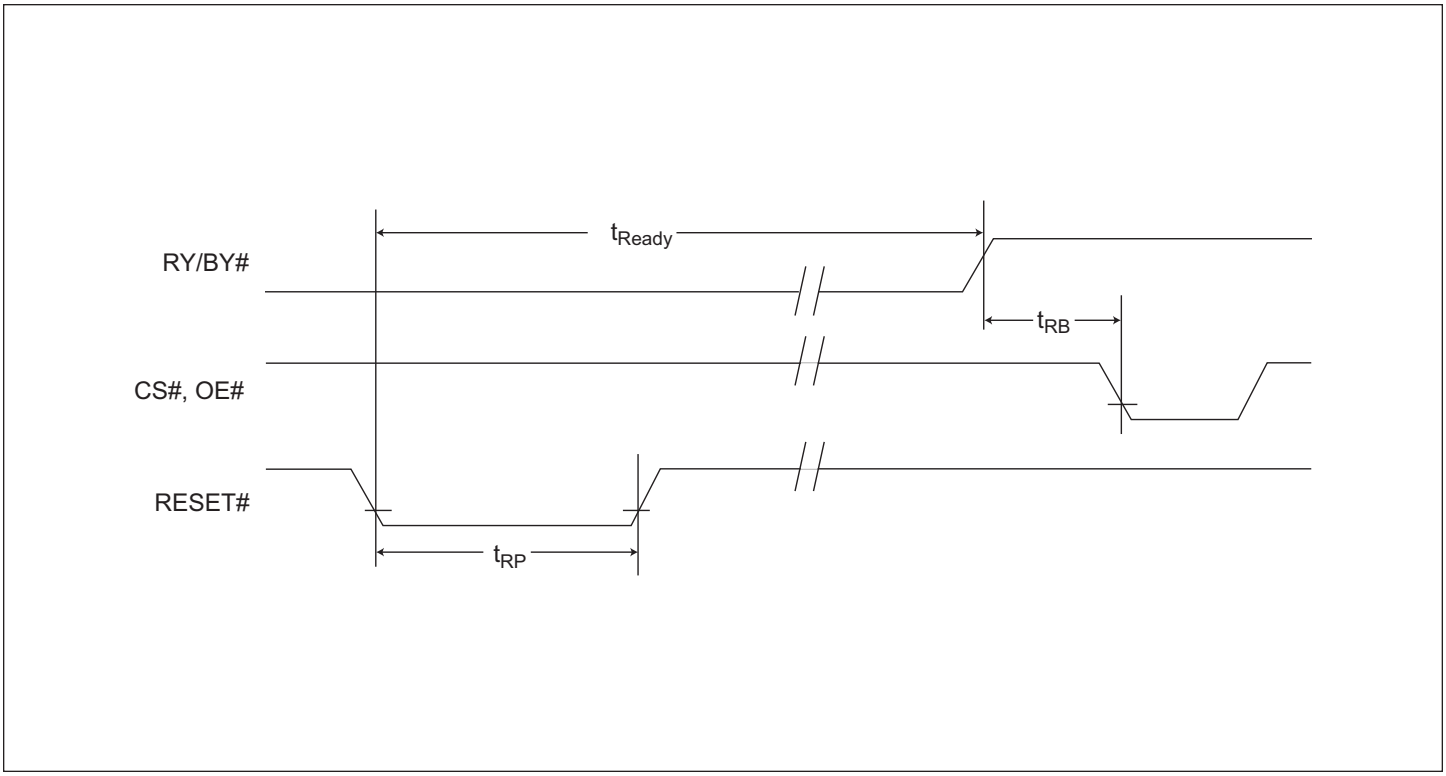


FIGURE 19 – POWER-UP SEQUENCE TIMINGS

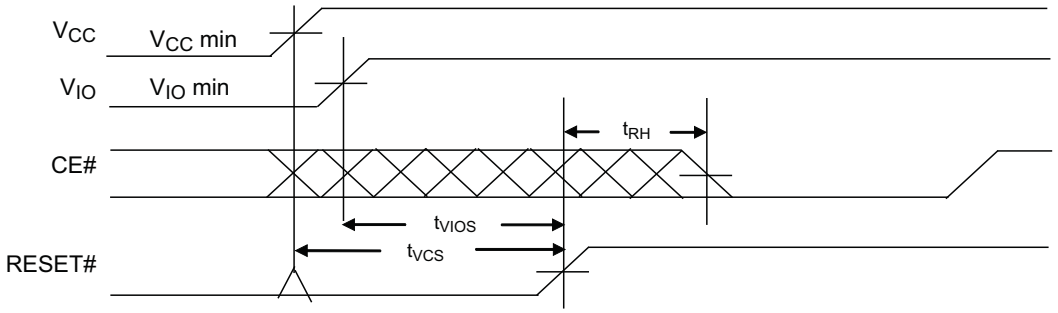
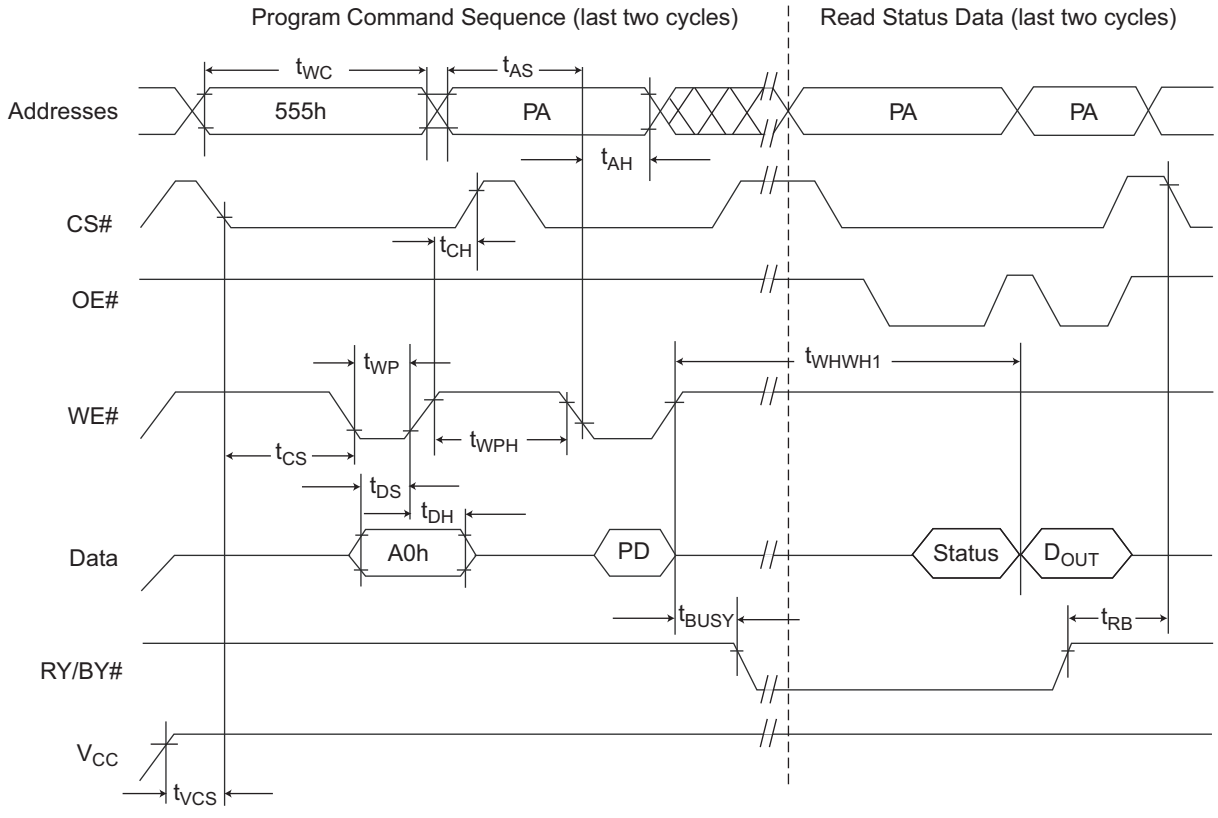
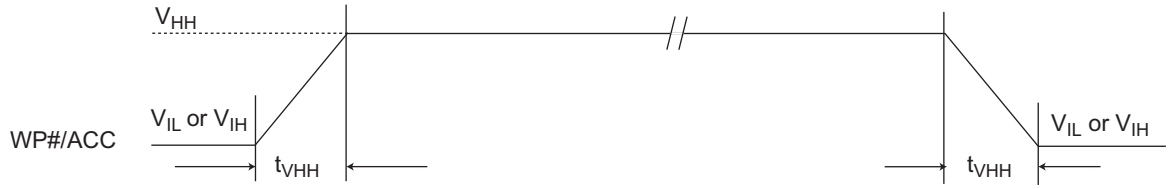


FIGURE 20 – PROGRAM OPERATION



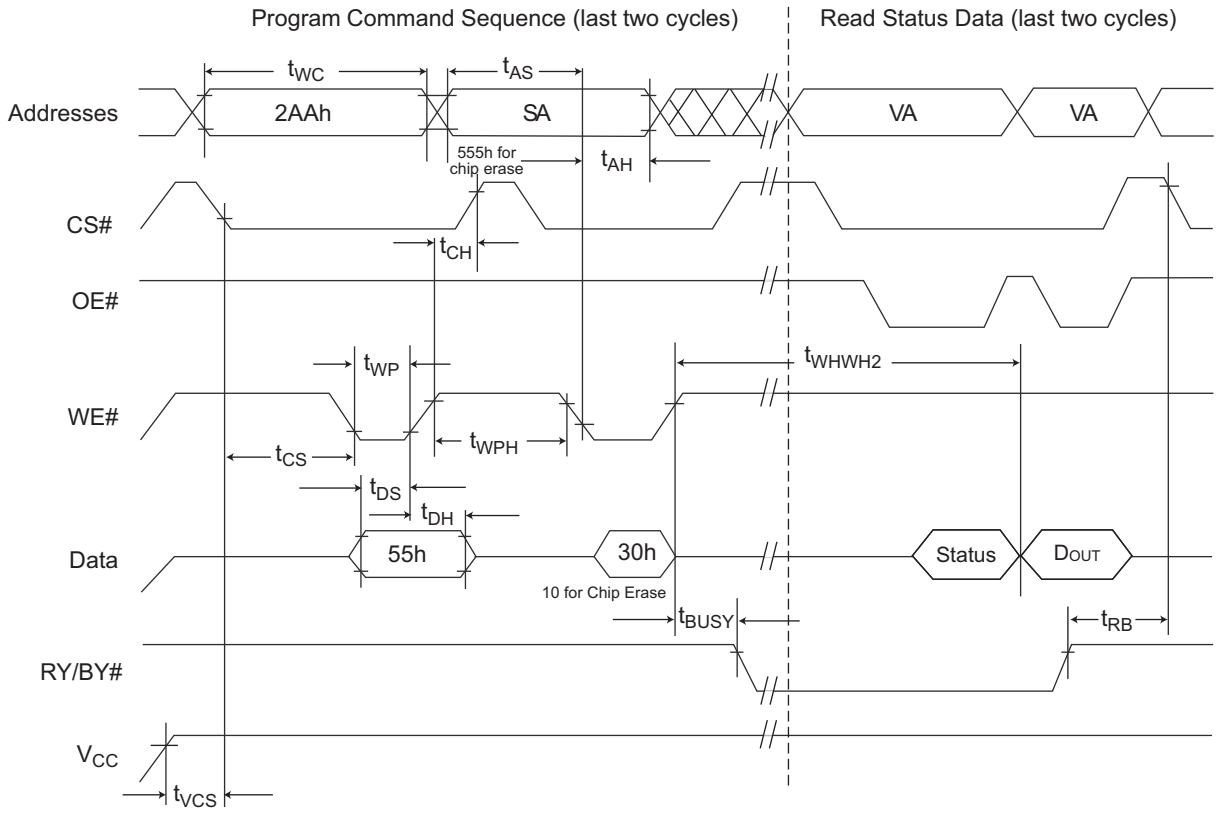
NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D_{OUT} is the output of the data written to the device.

FIGURE 21 – ACCELERATED PROGRAM TIMING DIAGRAM



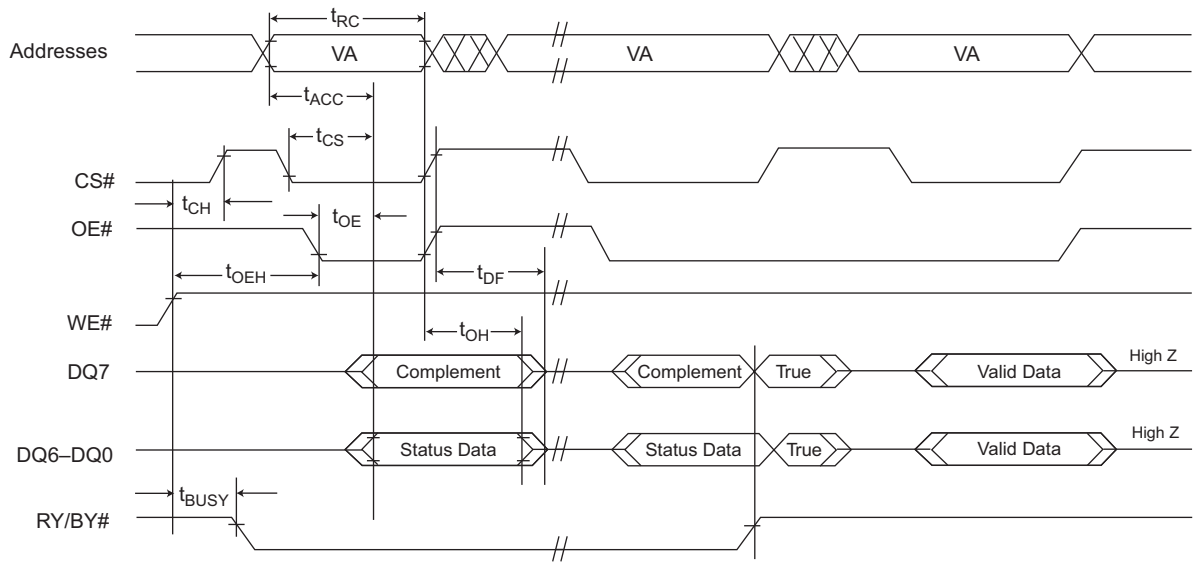
Notes:
1. Not 100% tested
2. CE#, OE# = V_{IL}
3. OE#, = V_{IL}
4. See figure 4 and Table 32 for test specifications

FIGURE 22 – CHIP/SECTOR ERASE OPERATION TIMINGS



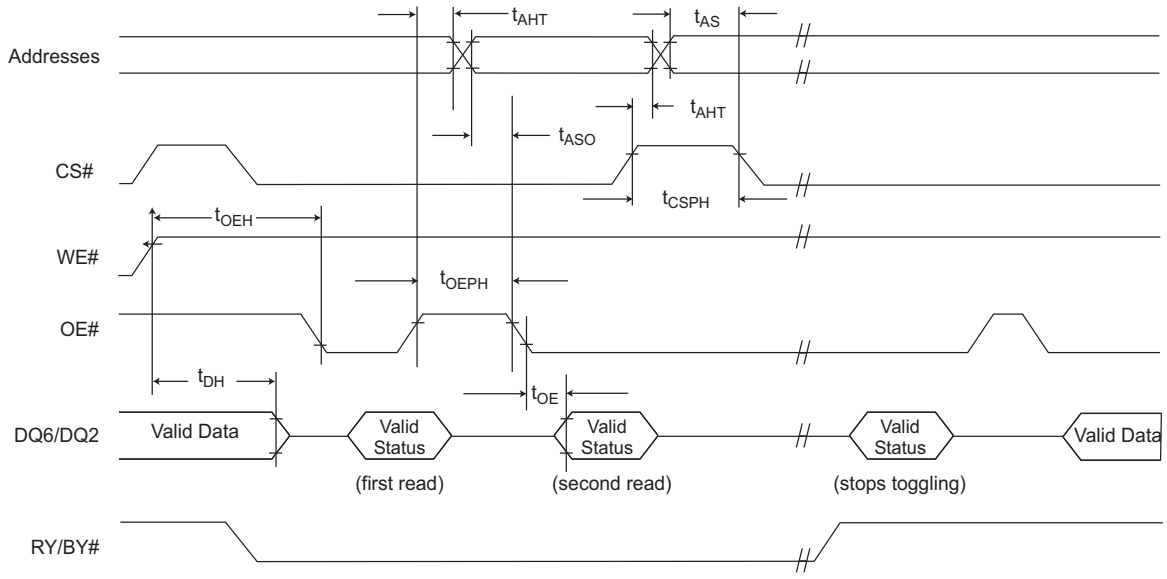
Notes:
1. SA = Sector Address (for Sector Erase), VA = Valid Address for reading status data (see "write operation status")
2. These waveforms are for word mode.

FIGURE 23 – DATA# POLLING TIMINGS (DURING EMBEDDED ALGORITHMS)



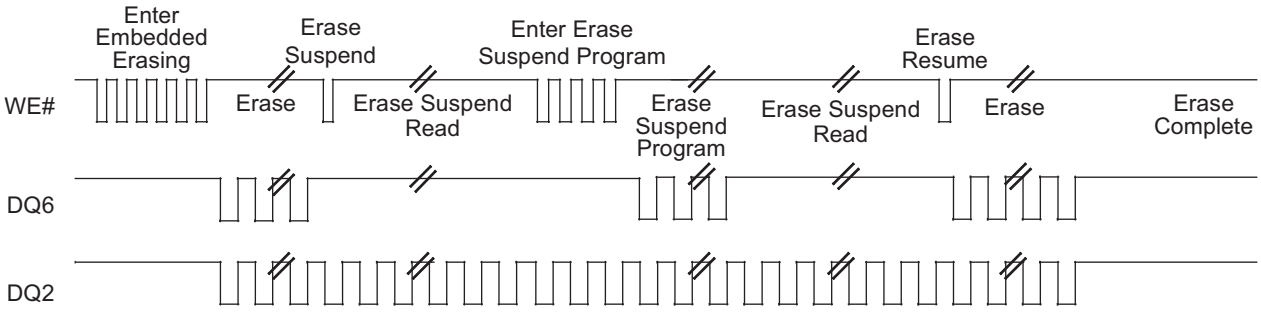
Notes:
1. VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.
2. T_{OE} for data polling is 35ns when V_{IO} = 2.7 to 3.6V.
3. CE# does not need to go high between status bit reads.

FIGURE 24 – TOGGLE BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



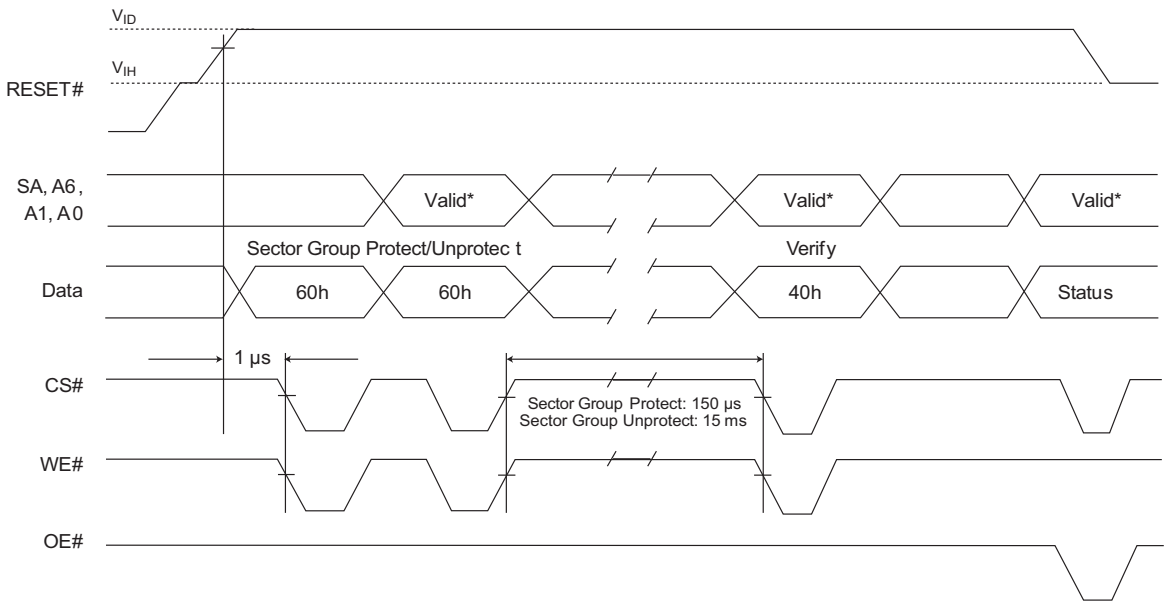
Note:
1. A = Valid address; Not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle
2. CE# does not need to go high between status bit reads.

FIGURE 25 – DQ2 VS. DQ6



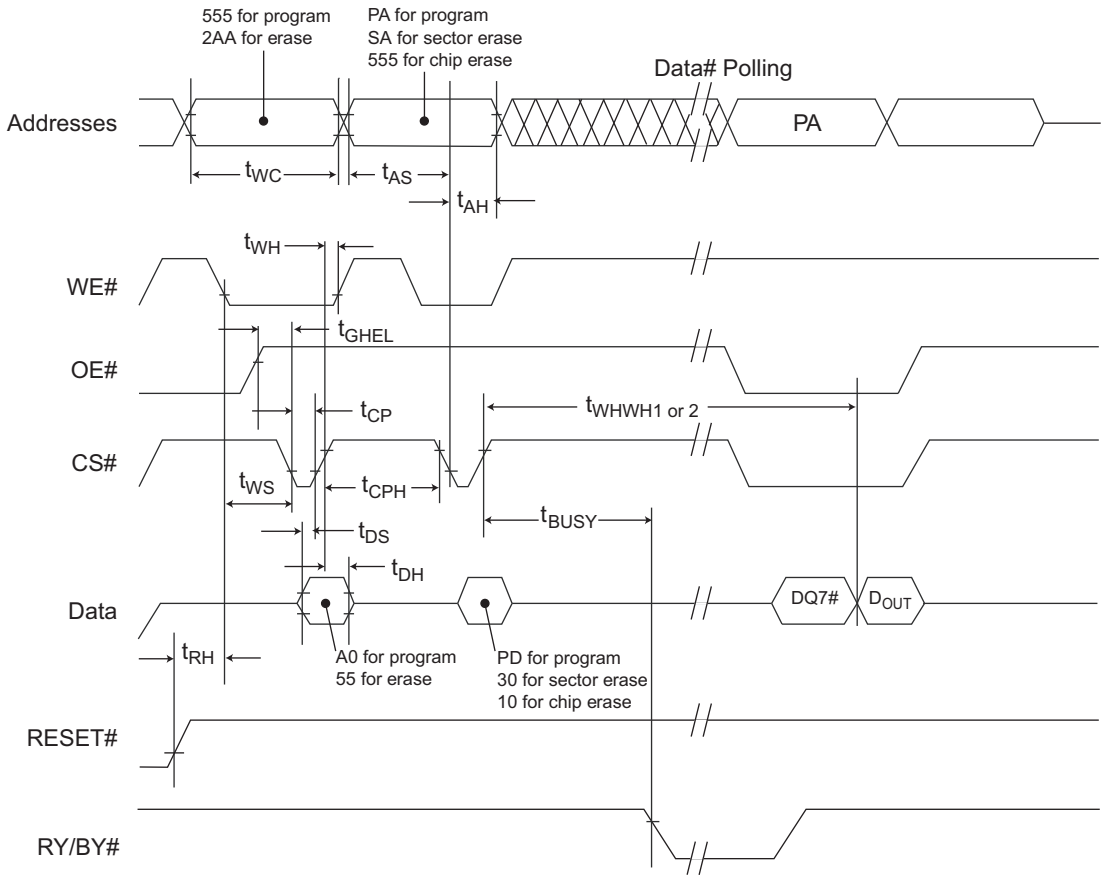
NOTE: DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CS# to toggle DQ2 and DQ6.

FIGURE 26 – SECTOR/SECTOR BLOCK PROTECT AND UNPROTECT TIMING DIAGRAM



NOTE:
For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.

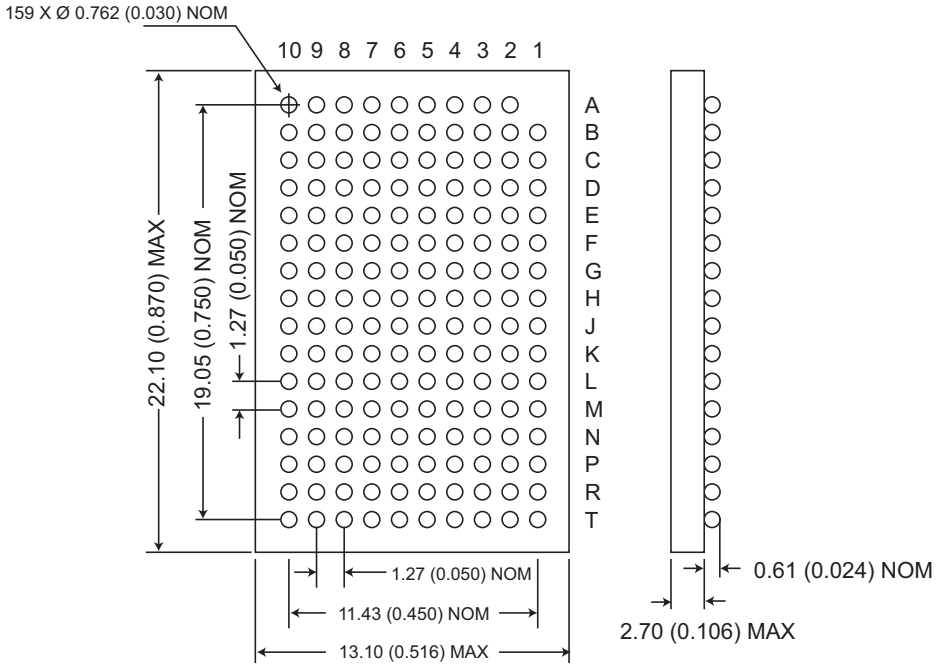
FIGURE 27 – ALTERNATE CS# CONTROLLED WRITE (ERASE/PROGRAM) OPERATION TIMINGS



NOTES:
1. Figure Indicated last two bus cycles of a program or erase operation.
2. PA = program address. SA = sector address, PD = program data.
3. DQ7 is the complement of the data written to the device. D_{OUT} is the data written to the device.

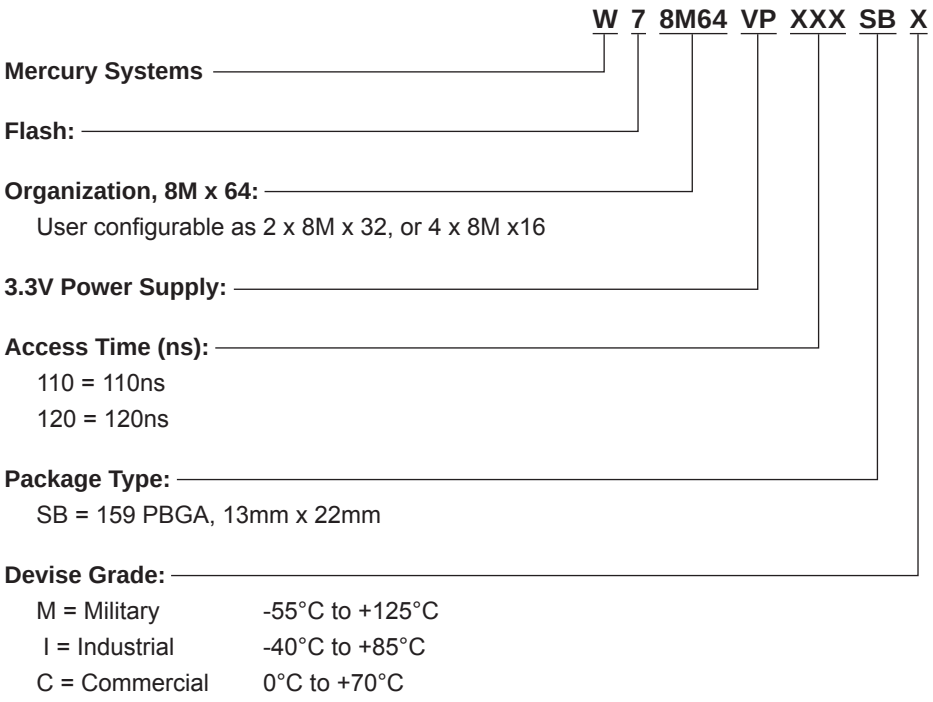
PACKAGE – 159 PBGA (PLASTIC BALL GRID ARRAY)

BOTTOM VIEW



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



Document Title

8Mx64 NOR Flash 3.3V Page Mode Multi-Chip Package

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	June 2008	Advanced
Rev 1	Change (Pg. All) 1.1 Add detail to DC, AC and programming sections	July 2008	Advanced
Rev 2	Change (Pg. 1, 3, 25, 27, 47) 2.1 Removed 90 and 100ns access times 2.2 Added 110ns access time	October 2008	Advanced
Rev 3	Change (Pg. 2) 3.1 Correct ball B6; change from "NC" to "DQ57"	December 2008	Advanced
Rev 4	Change (Pg. 2, 25, 26, 28) 4.1 Remove "TBD" from pin configuration and block diagram 4.2 In Table 30; I_{CC5} is 2mA 4.3 In Table 30; Add Note 3 to $I_{LI\ (WP/ACC)}$, I_{LIT}, I_{LOZ}, I_{CC6}, I_{ACC}, V_{HH}, V_{ID}, V_{LKO} 4.4 In Table 30; Remove $V_{IL} = V_{SS}$ + 0.3V/-1.0V from I_{CC6} and I_{CC5} 4.5 In Table 32; Remove Note 1 from read cycle time, page access time and output enable hold time 4.6 In Table 32; Change page access time to 25ns on both -100 and -120 4.7 In Table 35; Change output enable to output valid symbol to $t_{GLQ}V$ 4.8 In Table 35; Remove Note 1 from duration of byte programming operation 4.9 In Table 35; Remove Note 3 from write cycle time 4.10 Change 100 to 110 in Table 35 4.11 In Table 36; Remove Note 1 from write cycle time and correct JEDEC symbol t_{AVAV} 4.12 Add new page; Test Conditions - Figure 11 - Test Setup Diagram and Table 40 - Test Specifications 4.13 Update all figures and tables following addition of Figure 11 and Table 40	December 2008	Advanced
Rev 5	Change (Pg. 48) 5.14 Change dimension thickness to 2.70 (0.106) max due to typo	March 2009	Advanced

Document Title

8Mx64 NOR Flash 3.3V Page Mode Multi-Chip Package

Revision History (Continued)

Rev #	History	Release Date	Status
Rev 6	Change (Pg. 1, 2, 3, 16 ,23, 26, 30, 39, 41, 44) 6.1 Delete V_{IO} range is 1.65 to V_{CC} 6.2 Remove (*) astrisk from pin H10, A-1 from Fig 3, correct spelling of versatile in Fig. 2 6.3 Delete versatile IO (V_{IO}) control pargraph 6.4 Remove paragraph on customer programming services 6.5 Remove all reference to Fig. 8.1 6.6 Change output hold from address in Table 32 to 0 for both speeds grades, change output enable hold time - Read to 0 for both speed grades 6.7 Table 38, note 1 is Table 2, note 8 is Table3 6.8 Table 39 note 1 is Table 2 6.9 Correct Fig. 12; Maximum negative overshoot wave form, Fig. 13; maximum positive overshoot waveform 6.10 Add Table 40; Power-up sequence timings and notes	March 2009	Advanced
Rev 7	Change (Pg. 29) 7.1 Table 37 notes: change notes 1-5	June 2009	Advanced
Rev 8	Change (Pg. 4, 7,25, 26, 27, 28, 29, 30, 39, 40, 41, 43, 45, 46) 8.1 Change Table 38 to 39 8.2 Add new Table 32 - Test Specifications 8.3 Re-number table sequence from Table 32 8.4 Add Note #1 to Figure 16 8.5 Remove Table 41, duplicate to Table 35 8.6 Add Note #4 to Figure 21 8.7 Add Note #2 to Figure 24	August 2009	Advanced
Rev 9	Change (Pg. 1, 2, 17, 18, 19, 20, 21, 22, 23, 24, 25, 27) 9.1 Remove "/128KB sectors" from uniform sector architecture - No Byte mode 9.2 Remove "/256 byte and /16 byte" from secured silicon sector region. 9.3 Remove "under development, is not qualified or characterized and is" or cancellation. 9.4 Remove "Pin A-1" from block diagram 9.5 Remove "Byte# = V_{IL}" in device operations 9.6 Remove "AMax:A-1 in byte mode," from Notes in device operations 9.7 Remove all reference to "Byte Address" from pages 17 through 23 9.8 Change I_{LI} to 10µA for WP/ACC and 8µA for others, I_{LIT} = 70µA, I_{LO} = 2µA, I_{CC1} = 440µA, I_{IO2} = 20µA, I_{CC2} = 20µA, I_{CC3} = 180µA, I_{CC4} = 10µA, I_{CC5} = 1mA, I_{CC6} = 10µA, I_{ACC} = 40mA for WP#/A_{CC} Pin and 160mA for V_{CC} Pin 9.9 Add Note (1) to AC Characteristics: t_{OE} for data polling is 45ns when V_{IO} = 1.65V to 2.7V and 32ns when V_{IO} = 2.7V to 3.6V.	September 2009	Advanced

Document Title

8Mx64 NOR Flash 3.3V Page Mode Multi-Chip Package

Revision History (Continued)

Rev #	History	Release Date	Status
Rev 10	Change (Pg. 1, 23) 10.1 Remove “Advanced,” “under development, is not qualified or characterized and is,” “or cancellation.” 10.2 Add capacitance values to table 27. C_{WE} = 13pf, C_{CS} = 25pf, $C_{I/O}$ = 15, C_{AD} = 30pf, C_{RB} = 40pf and C_{OE} = 35pf. 10.3 Change status of data sheet to Final. 10.4 Change “max” to “22” 10.5 Remove “Note” in Fig. 16	October 2009	Advanced
Rev 11	Change (Pg. 26, 27) 11.1 Corrected Table 35 11.2 Add “t_{CH}” to Table 37	November 2009	Final
Rev 12	Change (Pg. 47) 12.1 Updated MO Drawing to 2.70 (0.106) max	March 2010	Final
Rev 13	Change (Pgs. 1-44) 13.1 Change document layout from White Electronic Designs to Microsemi	June 2011	Final
Rev 14	Changes (1, 41, 42, 43) 14.1 Add "NOR" to headline	August 2011	Final
Rev 15	Changes (Pg. All) (ECN 10156) 15.1 Change document layout from Microsemi to Mercury Systems	August 2016	Final
Rev 16	Changes (Pg. All) (ECN 10957) 16.1 Update data sheet with new Mercury logo	July 2018	Final