# EnsembleSeries<sup>™</sup> HDS6602

6U OpenVPX dual Intel Xeon (Ivy Bridge) processing blade

- Dual Intel® 1.9GHz 10-core Xeon® (Ivy Bridge server-class) processors
- Up to 128 GB DDR3-1866 SDRAM
- 40 Gigabit Ethernet or InfiniBand switch fabrics
- Gen3 PCIe co-processing and I/O expansion plane communications
- Optional built-in BuiltSECURE System Security Engineering

# The EnsembleSeries<sup>™</sup> HDS6602 OpenVPX<sup>™</sup> blade embeds two of the latest generation of server-class Ivy Bridge 10-core Intel Xeon processors for the most compute intense applications.

Each EnsembleSeries HDS6602 blade combines this processing performance with the new Mellanox ConnectX-3 high-speed bridge, scaling the module's I/O infrastructure to match the embedded processing performance of server-class Intel processors. By leveraging the power of Intel server-class processing in combination with the on-board integrated high performance PCle and fabric infrastructure, the HDS6602 delivers a balanced and scalable computing architecture, capable of providing the processing power required for complex on-platform processing including sensor fusion and artificial intelligence in a standard 6U OpenVPX form factor.

# **Optional BuiltSECURE**

For deployment at the tactical edge and export to allies, EnsembleSeries HDS6602 blades optionally embed BuiltSECURE technology to counter nation-state reverse engineering with system security engineering (SSE). BuiltSECURE is built-in SSE that enables turnkey or private and personalized security solutions to be quickly configured. The extensible nature of Mercury's SSE delivers system-



Mercury Systems is a leading commercial provider of secure sensor and safety-critical processing subsystems. Optimized for customer and mission success, Mercury's solutions power a wide variety of critical defense and intelligence programs. wide security that evolves over time, building in future proofing. As countermeasures are developed to offset emerging threats, Mercury's security framework keeps pace, maintaining system-wide integrity. Please contact Mercury directly for BuiltSECURE configurations.

# Intel Xeon Sandy Bridge Server-Class Processor

EnsembleSeries HDS6602 blades features two 64-bit Xeon (E5-2648L v2, Ivy Bridge) 10-core processors. Leveraging fabrication capabilities first deployed for the EnsembleSeries HDS6601 and HDS6600, the HDS6602 transforms the two instances of 2011-pin Land Grid Array (LGA) processors to Ball Grid Arrays (BGAs) in a rugged, embedded form-factor. The dual 10-core processors are linked via two instances of the high-speed, low-latency QPI interface, each provides 32 GB/s transfer rates, for a total of 64 GB/s of bandwidth between processors.

This interconnected processor architecture is optimized for the data movement needed by high-performance processing algorithms, such as all-to-all corner turn operations. From a software perspective, this QPI architecture allows the EnsembleSeries HDS6602 to be configured with a single kernel NUMA-aware operating system running across both processor devices. Each processor is capable of delivering approximately 304 GFLOPS (peak), with four high-speed, 14.9 GB/s DDR3-1866 memory channels raw bandwidth each, for a total peak performance of 608 GFLOPS and 119.4 GB/s total raw memory bandwidth.





EnsembleSeries HDS6602 blades refine the innovative standing memory technology first seen on the HDS6600 and HDS6601 to support up to 128 GB of DRAM on-board. Native Gen3 PCIe support is also featured on this processor, linking the processing resources directly to the I/O sources on the blade. The HDS6602 also makes use of the Patsburg-B platform controller hub (PCH) chipset, which provides additional I/O bridging between the Intel processor and external devices.

Each Intel E5-2648L v2 processor includes a large 25 MB cache, shared between the cores, allowing many high-performance calculations to remain cache resident. This accelerates processing by eliminating the potential latency required to access DRAM to fetch upcoming data. The Ivy Bridge family of processors support the proven AVX instruction set, delivering an increase in floating-point algorithm performance that is portable to future Intel architectures.

# High Speed Fabric Interfaces

EnsembleSeries HDS6602 blades joins the LDS6523 as one of the first embedded processing blades to utilize dual Mellanox ConnectX-3 host adaptors for data plane communications. Bridging between the native Gen3 PCle interfaces on the Intel processors and the OpenVPX data plane, the ConnectX-3 can be configured to support InfiniBandTM (DDR at 5Gbaud, QDR or FDR10 at 10Gbaud) or 40 Gb/s Ethernet as the data protocol. This advancement scales the data plane bandwidth to up to a peak theoretical rate of up to 4 GB/s per port, or 16 GB/s aggregate across the entire four-port OpenVPX data plane. By scaling the data plane bandwidth to match the increase in processing performance, the HDS6602 architecture ensures that the processor is never starved for data.

EnsembleSeries HDS6602 blades are compliant to the VITA 65 module profile MOD6-PAY-4F102U2T-12.2.1-n, where n can vary based on ConnectX-3 configuration. The HDS6602 is supported in chassis slots compliant with VITA 65 slot profile SLT6-PAY-4F102U2T-10.2.1.

# PCIe Architecture

EnsembleSeries HDS6602 provides high-end Gen3 PCIe backplane interfaces via the native PCIe resources on the Intel E5-2648L v2 processors. In addition to supporting the processor's interface to the ConnectX-3 bridges, an additional x16 Gen3 PCIe interface is provided to the OpenVPX expansion plane interface on both the P2 and P5 VPX connectors. These interfaces enable the HDS6602's compatibility with Mercury's GPU, FPGA, or mezzanine carrier modules. The interfaces are user configurable to lower port widths, and may also support non-transparent (NT) bridge functionality at run time. These configuration options support the construction of complex PCIe trees with many other PCIe-capable devices.

	Module I/O				
	Air-cooled		Conduction-cooled	Air Flow-By	
	Front Panel	Backplane	Backplane	Front Panel	Backplane
InfiniBand		DDR/QDR/FDR10*	DDR/QDR/FDR10*		DDR/QDR/FDR10*
Or Ethernet		4 x AUI (10Gb)*	4 x AUI (10Gb)*		4 x AUI (10Gb)*
USB 3.0					
USB 2.0		2	2		2
Gen 3 PCIe (8x)		32 - Dual full x16 or dual x8	32 - Dual full x16 or dual x8		32 - Dual full x16 or dual x8
1000BASE-T Gigabit Ethernet	1 (RJ45)	1	2	1 (RJ45)	1
1000BASE-BX SERDES Ethernet		2	2		2
SATA	1 x eSATA	2	2		2
RS232/RS422	1 x RS-232 (µDB9)	1 x RS-422 2 x RS-232	1 x RS-232 or RS-422 1 x RS-422 2 x RS-232	1 x RS-232 (µDB9)	1 x RS-422 2 x RS-232
IPMB-A & IPMB-B link		1	1	1	

\* 40 Gb/s option coming soon

# System Management

EnsembleSeries HDS6602 blades implements the advanced system management functionality architected in the OpenVPX specification to enable remote monitoring, alarm management, and hardware revision and health status.

Using the standard I2C bus, intelligent platform management controller (IPMC), and IPMI protocol, the on-board system-management block implementation is VITA 46.11 compliant. This allows the HDS6602 blades to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage, or current variations that exceed those thresholds
- Reset the entire blade
- Power up/down the entire blade
- Retrieve module field replaceable unit (FRU) information
- Be managed remotely by a chassis management controller at the system level, such as implemented on the EnsembleSeries SFM6104 switch
- Additional Features

Each HDS6602 blade provides all the features typically found on a single-board computer. In addition to the sophisticated management subsystem and fabric interconnect, HDS6602 blades provide users with a toolkit enabling many different application features including:

- Thermal and voltage sensors integrated on-board
- Real-time clock with granularity to 1ms and time measurement of up to 30 years
- General purpose timers
- Global clock synchronization capabilities via the OpenVPX utility plane clock signals
- Watchdog timer to support interrupt or reset
- Multiple boot paths, include netboot, USB boot, boot from SATA, or from the on-board 8GB flash device

# **Open Software Environment**

Mercury leverages over 35 years of multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the EnsembleSeries HDS6602 blade. The same Linux<sup>®</sup> development and run-time environment is implemented on the HDS6602 as on other Intel-based EnsembleSeries 3000 and 6000 building blocks. Off-the-shelf open software such as OFED and OpenMPI are fully supported by the Mellanox ConnectX-3 data plane.

# System bandwidth - the effect of interconnect performance

Bandwidth is critical and especially applicable to switched fabric resources, which dictate the responsiveness of the entire subsystem. All modular solutions, including OpenVPX are to some degree or another, interconnect-bound; they are restricted by the limitations of the best industry interconnect technology. To address this, Mercury fabricates system interconnections with innovative technology, which mitigates insertion-loss and cross-talk while maintaining full VITA/OpenVPX compliance. The resulting and significant system performance boost is especially discernible as subsystems scale larger.

# Mercury Sensor Processing Ecosystem

Modern sensor compute subassemblies are customized assemblies of interoperable building blocks built to open standards. Mercury's hardware and software portfolio of building blocks are physically and electrically interoperable as defined by international industrial standards, including VITA's OpenVPX standards. Mercury subsystems are designed from a suite of sophisticated open architecture building blocks that are combined and scaled to meet a broad range of advanced sensor chain processing requirements.

Mercury subsystems may include analog, digital and mixed-signal receiver modules, single-board computers and signal processing payload modules. Payloads may have acquisition, digitization, processing, and exploitation and dissemination elements and include FPGA, CPU, GPU or ADC/DAC technology, and be made up of multiple subsystems developed to multiple standards, including OpenVPX and others such as ATCA, ATX/E-ATX, or VME/VXS.



Figure 2. HDS6602 functional block diagram

### Module packaging

#### **VPX-REDI**

The VPX (VITA 46) standard defines 6U and 3U board formats with high performance interconnects capable of supporting today's high-speed fabric interfaces. VPX may be paired with the ruggedized enhanced design implementation standard — REDI (VITA 48). HDS6602 blades when implemented as conduction-cooled or Air Flow-ByTM are VPX-REDI compatible. Air-cooled equivalents conform to the same OpenVPX form factor and are suitable for less challenging environments. Targeted for harsh embedded environments, VPX-REDI supports higher functional density and two-level maintenance (2LM). 2LM allows relatively unskilled maintenance personnel to replace a failed module.

#### Rugged air cooling, Air Flow-By

Air- and conduction-cooled subsystems rely on filtration to remove contaminants from their cooling air streams. Mercury's Air Flow-By technology eliminates filtration with the most elegant cooling solution available within a sealed and rugged package. Fully compliant to the VITA 48.7 standard, Air Flow-By maintains OpenVPX's 1-inch pitch requirement, is highly resilient to liquid and particle contamination, boosts SWaP, reduces operating temperature, extends MTBF by an order of magnitude and enables embedded deployment of the most powerful and reliable processing solutions.

HDS6602 modules are available as air-cooled (various levels of ruggedness), and rugged Air Flow-By and conduction-cooled variants.

# **Specifications**

#### Intel 3<sup>rd</sup> Generation Xeon 10-Core Processor

Intel 3rd Generation Xeon 10-Core processor

 Dual Intel 1.9GHz 10-core E5-2648L v2 (22nm Ivy Bridge) server-class processors

 Peak performance
 608 GFLOPS

 Threads per core:
 2

 QPI interface between processors:
 2 x 8 GT/s

 (or 32 Gb/s per processor, per direction) peak performance

Intel Virtualization Technology Dual Integrated x16 Gen3 PCle interface

#### Memory

Up to 128 GB DDR3-1866 with ECC Raw memory bandwidth: 59.7 GB/s per processor

#### BIOS

SPI flashDual 8 MB partitionsNAND flash8 GB, SATA interface

#### **Data Plane PCIe to Switched Fabric Bridge**

Mellanox ConnectX-3 VPI host adapter Support DDR, QDR, or FDR10 InfiniBand or 40 Gb/s Ethernet protocols

#### **Ethernet Connections**

Ethernet functions supported by the chipset include:

UDP, TCP, SCTP, ARP, IPv4, IPv6, IEEE1588, flow control, 802.1P (priority) and 802.1Q (VLAN)

#### Intelligent Platform Management Interface (IPMI)

On-board IPMI controller Voltage and temperature monitor Geographical address monitor Power/reset control FRU and on-board EEPROM interfaces FPGA, CPU, and CPLD interfaces

#### **OpenVPX Multi-Plane Architecture**

System Management via IPMB-A and IPMB-B link on PO management plane InfiniBand or 40 Gigabit Ethernet interfaces on data plane Dual full x16 or dual x8 PCIe Gen3 expansion plane Dual 1000BASE-BX Ethernet control plane

#### **Mechanical**

6U OpenVPX 1.0" slot pitch OpenVPX and VPX REDI

#### Compliance

OpenVPX (VITA 65) encompassing: VITA 46.0, 46.3, 46.4, 46.6, 46.11, and VITA 48.1, 48.2 (REDI) VITA 65 module profile MOD6-PAY-4F102U2T-12.2.1-n (where n can vary based on ConnectX-3 configuration) Compliant with VITA 65 slot profile SLT6-PAY-4F102U2T-10.2.1.

PCIe, 10 Gigabit Ethernet

Please refer to Mercury publication "Environmental Protections for Operation at the Tactical Edge" for specific ruggedness levels and cooling options.

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