PBGA THERMAL RESISTANCE CORRELATION

INTRODUCTION

The thermal resistances for the Plastic Ball Grid Array (PBGA) Multi Chip Packages (MCP) published in WEDC data sheets are results from thermal modeling software calculations. This paper explains how the simulation results were correlated to actual measured values.

DEFINITIONS

P_D (W) =Total package power dissipation

T_J (°C) =Junction Temperature

T_A (°C) = Ambient Temperature

T_T (°C) = Top case Temperature

T_B (°C) = Board Temperature

θ_{JB} (°C/W) = Junction to Board thermal resistance defined as $(T_J - T_B)/ P_D$

θ_{JC} (°C/W) = Junction to Case thermal resistance defined as $(T_J - T_C)/ P_D$

θ_{JA} (°C/W) = Junction to Ambient thermal resistance defined as $(T_J - T_A)/ P_D$

Ψ_{JT} (°C/W) = Junction to Top case thermal resistance defined as $(T_J - T_T)/ P_D$

SCOPE

The thermal modeling software was specifically designed for silicon packages such as these multi-chip PBGAs. The thermal modeling uses design entries such as mechanical dimensions, die placement and thickness, thermal material properties, ball amount and placement, etc. The calculations provide three thermal resistances that are used in user's applications to determine maximum junction temperature, and then the need to use cooling techniques if necessary. The three thermal resistances are Junction to Ambient (θ_{JA}), Junction to Board (θ_{JB}), and Junction to Case (θ_{JC}) thermal resistance as defined per JEDEC JESD51 specifications.

Note: Junction to Top case thermal resistance (Ψ_{JT}) is not provided since by definition top case temperature is taken at the top center of the package. Since these MCPs usually do not have die in the center it doesn't represent worst case. The maximum Junction to Case thermal resistance (θ_{JC}) of the die with the biggest resistance value is published.

CALIBRATION, MEASUREMENTS AND MODELING

The WEDPN8M72V-XBX SDRAM device was chosen as the test vehicle since it is represents a typical large BGA package. The device is a multi-chip plastic BGA package that contains five 128Mb SDRAM memory die. External dimensions are 25mm x 32 mm with 219 balls on a 1.27mm pitch. See mechanical Outline per figure 1.

Using JEDEC JESD51 specification method, the devices were mounted on a 101.60 x 114.30mm 1.60mm thick 4-layer board (see Figure 2).

Actual production devices with functional die (vs. thermal die) were used for test, where the parallel combination of the Vcc/Gnd reversed bias of all die were utilized as the heating source.

Calibration: The forward-voltage drop of the parallel combination of Vcc/Gnd reversed bias of the chips was used as the temperature sensitive parameter. The electrical method of junction temperature measurement is based on a temperature and voltage dependency exhibited by all semiconductor diode junctions. This relationship, often referred to as the Temperature Sensitive Parameter (TSP) slope can be measured and used to compute the semiconductor junction temperatures in response to power dissipation in the junction region. These measurements were performed in a dielectric oil bath under unpowered, thermal equilibrium conditions so junction and case temperature are nearly equal.

Measurements: Temperature measurements were performed per JEDEC JESD51 specifications on 10 devices. Using equations from definitions, the thermal resistance was calculated:

- θ_{JA} had an average of 13.3°C/W with a maximum of 13.9°C/W
- θ_{JB} had an average of 8.8°C/W with a maximum of 9.2°C/W
- Ψ_{JT} had an average of 1.3°C/W with a maximum of 1.9°C/W

Modeling Results:

- θ_{JA} = Average 13.96 °C/W with a maximum of 14.3°C/W
- θ_{JB} = Average 9.93 °C/W with a maximum of 10.4°C/W
- Ψ_{JT} = Average 2.17 °C/W with a maximum of 2.6°C/W

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CONCLUSIONS

The software modeling calculates the worst case thermal resistance for each die depending on the module design. The measurements were performed on typical production devices using the JEDEC thermal measurement method.

The measured values on this device were within 10% for θ_{JA} and 15% for θ_{JB} . The differences in Ψ_{JT} results were further apart in percentage, but less than 1°C/W lower than the modeling and are explained by the short distance and the small temperature difference between the top of the die (junction) and the case temperature.

These results, for all three measured thermal resistances, correlate the modeling calculations and validates the correctness of the models.

Figure 1 – Package Dimension: 219 Plastic Ball Grid Array (PBGA)

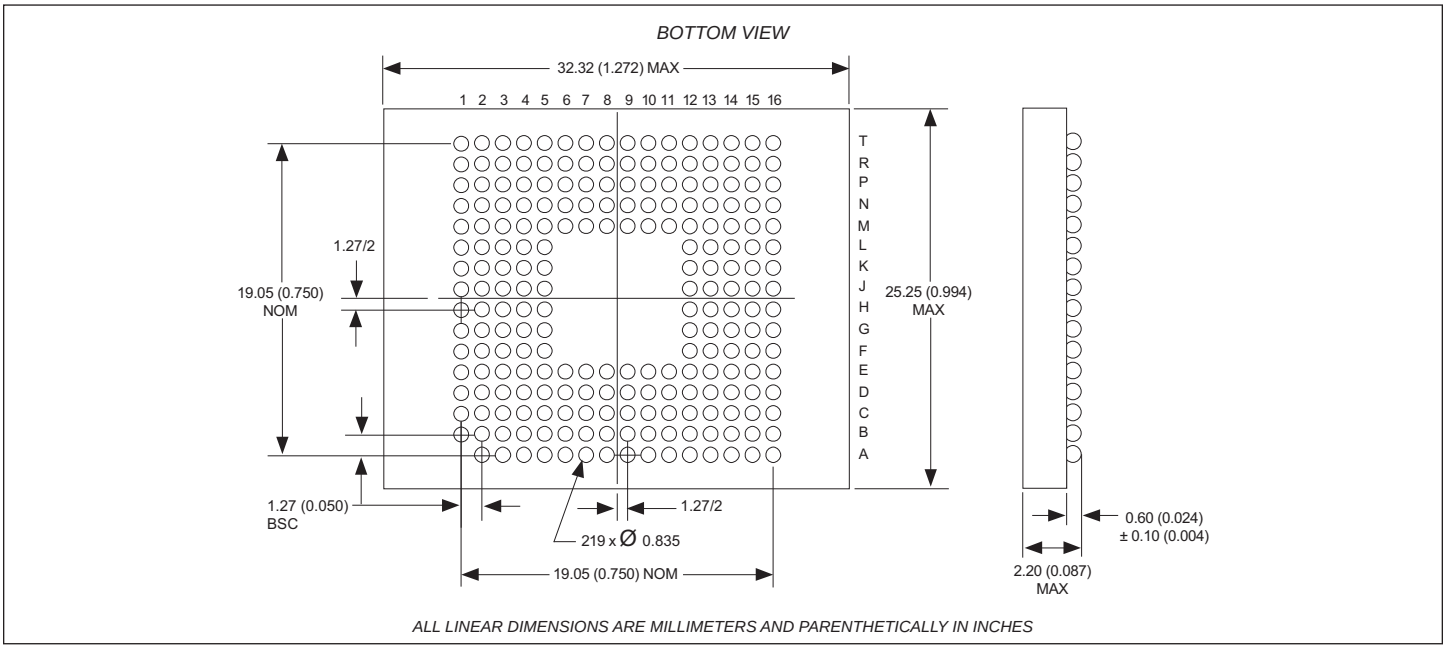
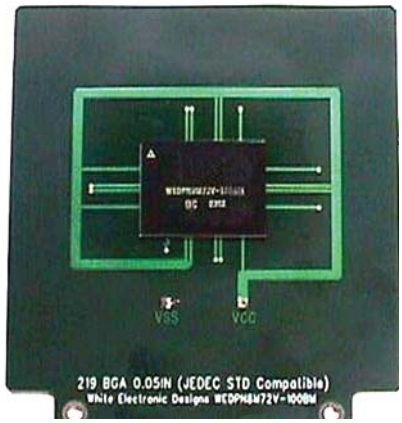


Figure 2



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