The EnsembleSeries™ LDS3517 blade combines Intel’s Xeon D family of server-class processors with Xilinx’s UltraScale family of FPGA devices in the flexible 3U OpenVPX form factor. This dense union of best available commercial-item general processing and FPGA resources produces a highly versatile, affordable and interoperable building block for embedded, high-performance compute applications with optional BuiltSECURE foundation required to support a wide variety of mission capabilities. When paired with the I/O flexibility of an on-board XMC mezzanine site, the LDS3517 represents a flexible solution to a wide variety of signal and mission processing requirements.

The Xilinx’s UltraScale FPGA provides a platform for Mercury and third party IP and enables offload of protocol translation and embedded security functions. By leveraging the built-in FPGA functional elements in combination with Mercury’s extensive software and FPGA IP library, the EnsembleSeries LDS3517 becomes a balanced and affordable building block for mission and sensor processing applications with tight SWaP budget.

Optional MOTS+

The EnsembleSeries LDS3517 family of blades has options for modified off the shelf plus (MOTS+) packaging for extreme durability. MOTS+ configurations leverage enhanced commercial components, board fabrication rules, and subsystem design techniques for extra ruggedness and withstand extreme temperature cycles better than other rugged designs. Please contact Mercury directly for MOTS+ configurations.

Optional BuiltSECURE

For deployment at the tactical edge and export to allies, the EnsembleSeries LDS3517 family of blades optionally embeds BuiltSECURE technology to counter nation-state reverse engineering with system security engineering (SSE). BuiltSECURE is built-in SSE that enables turn-key or private and personalized security solutions to be quickly configured. The extensible nature of Mercury’s SSE delivers system-wide security that evolves over time, building in future-proofing. As countermeasures are developed to offset emerging threats, Mercury’s security framework keeps pace, maintaining system-wide integrity. Please contact Mercury directly for BuiltSECURE configurations.

SOSA profiles

EnsembleSeries LDS3517 is optionally available in Sensor Open Systems Architecture (SOSA) compatible configurations.

Mercury Systems is the better alternative for affordable, secure processing subsystems designed and made in the USA. These capabilities make us the first commercially based defense electronics company built to meet rapidly evolving next-generation defense challenges.
Intel Xeon D Family Server-Class Processor

EnsembleSeries LDS3517 blades feature a 64-bit Xeon D processor, cooled by Mercury’s wide selection of enhanced packaging, which has previously been deployed with the EnsembleSeries LDS3506 and other 3U and 6U modules. Mercury’s module design elegantly allows cooling technologies to be deployed with no change to the underlying module assembly, giving the LDS3517 the ability to support the VITA 48 standard suite of convection, conduction, and Air Flow-ByTM or Air Flow Through standards without changes to the underlying circuit board assembly.

The Xeon D family of Intel processors delivers a system chip (SoC) approach, combining the processor and the Intel platform controller hub (PCH) function within a single device. As a solderable BGA, the Xeon D family extends the applicability of the Xeon family into the compact 3U form-factor. As an example, the default CPU configuration of the D-1539 device delivers up to 410 GFLOPS of single precision processing power, which is a significant performance boost compared with previous generations. With two high-speed DDR4 memory controllers, the Xeon processor is able to support up to 16 GB of DRAM across two memory controllers, with future capabilities of up to 32 GB per blade. Significant PCIe interface capabilities are built in to the chip, which enable data interfaces both on-board and off-board.

The on-device PCH functionality enables the EnsembleSeries LDS3517 to access additional I/O, including USB and SATA on the backplane. Each LDS3517 blade leverages the processor’s built-in dual 10 Gb/s Ethernet interfaces to provide control plane functionality, optionally passed through the on-board FPGA to enable gatekeeping or packet inspection. The CPU also provides support for the AVX 2.0 instruction set. This boosts floating-point algorithm performance and is portable to future Intel architectures. The EnsembleSeries LDS3517 supports standard libraries for signal processing available in the industry as well as Mercury’s optimized MathPack, which allows users to select the highest performant algorithms from across the industry for a particular function and data size.

Integrated FPGA Resources

LDS3517 blades integrate a Xilinx UltraScale FPGA device with the Intel processor to provide additional payload functionality security offload capabilities. Embedded deeply within the LDS3517 boot and application load architecture, the FPGA provides many features independent of the CPU, such as serial interfaces, watchdog timers, and GPIOs to the backplane. By offloading traditional SBC functionality, the EnsembleSeries LDS3517 blade reduces DMS concerns for long-term support of program requirements. Mercury’s FPGA development kits are available and support the integration of customer or third party FPGA IP, and facilitate customer IP development efforts.

High-Speed Fabric Interfaces

A full Gen3 x8 PCIe interface is routed from the Intel CPU to the OpenVPX data plane. This interface is capable of being bifurcated into dual x4 interfaces, and can support lower speeds as well if necessary. The PCIe interface is ideally suited for board-to-board communication, interface to external I/O resources, or control of compute offload devices, such as GPGPUs.

EnsembleSeries LDS3517 blades support an additional Gen2 x4 PCIe expansion plane interface to integrate additional 3U modules, including those implementing mezzanine carriers, FPGA processing, and analog to digital conversion functions.

Mezzanine Card Flexibility

LDS3517 blades provide a single XMC mezzanine site. The standard mezzanine site may be configured with off-the-shelf mezzanine cards for additional I/O and processing options. XMCs are supported with x8 PCIe on the Jn5 connector per the VITA 42.3 standard. User I/O is mapped in the X8D+12D pattern to the backplane via the Jn6 XMC connector.

Each LDS3517 blade utilizes VITA 61 XMC 2.0 connectors in support of Gen3 PCIe signal integrity and greater ruggedness.

Multiple I/O Options

The EnsembleSeries LDS3517 includes a variety of additional built-in I/O options:

- A 10/100/1000BASE-T Ethernet connection routed to the backplane via on-board transceiver
- A single RS-422 serial interface is routed to the backplane P2 connector

![Figure 1 - LDS3517 functional block diagram](image-url)
• Two RS-232 serial ports are routed to the backplane P2 connector
• Backplane USB and SATA interfaces are provided for interfacing to I/O or storage devices as needed
• Multiple GPIO lines act as discrete I/O, usable as I/O or to generate interrupts on the blade
• Multiple additional bused signals enhance the functionality of the LDS3517 blade

System Management Plane
The LDS3517 blade implements the open and advanced system management functionality architected in the OpenVPX standard to enable remote monitoring, alarm management, and hardware revision and health status.

Using the standard I2C bus and IPMI protocol, the on-board system-management block implements the intelligent platform management controller (IPMC), in accordance with the VITA 46.11 standard. This enables the EnsembleSeries LDS3517 blade to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage, or current variations that exceed those thresholds
- Reset the entire blade
- Power up/down the entire blade
- Retrieve field replaceable unit (FRU) information
- Be managed remotely by a standard VITA 46.11-compliant chassis management controller

Additional Features
The EnsembleSeries LDS3517 provides all the features typically found on a single-board computer, sophisticated subsystem management and fabric interconnect. Each blade includes a toolkit to manage:

- Thermal and voltage sensors integrated on-board
- Real-time clock with granularity to 1ms and time measurement of up to 30 years
- General-purpose timers
- Global clock synchronization capabilities via the OpenVPX utility plane clock signals
- Watchdog timer to support interrupt or reset
- Multiple boot paths, include netboot, USB boot, or boot from external SATA

Open Software Environment
Mercury leverages over 35 years of multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the EnsembleSeries LDS3517 blade. Because the processor, memory, and surrounding technologies are leveraged across product lines, software developed on the LDS3517 blade can interface seamlessly with other Mercury modules. The same development and run-time environment is implemented on the EnsembleSeries LDS3517 blade as on other Mercury platforms across the EnsembleSeries 3000, 5000, and 6000 series.

Specifications

Main processor
Intel 8-core, 64 bit, Xeon D-1539
410 GFLOPS peak performance
AVX 2.0
Additional configurable processor SKUs
Xeon D-1548, Xeon D-1559

XMC
PCIe XMC sites per VITA 42.3 with XMC user-defined I/O from Jn6 to backplane
VITA 61 XMC 2.0 connectors
X8d+12D backplane user I/O

FPGA
Xilinx UltraScale XCKU095
BOM option to pass 10GBASE-KR interfaces through FPGA
Configurable GPIO from FPGA to backplane

System Memory
16 GB DDR4-2133 (32 GB planned)

Mechanical
3U OpenVPX
Blade packages:
VITA 48.1 Air-cooled
VITA 48.2 Conduction-cooled
VITA 48.7 Air Flow-By
VITA 48.8 Air Flow Through

Compliance
OpenVPX System Specification (VITA 65) encompasses:
VITA 46.0, 46.3, 46.4, 46.6, 46.11, and VITA 48.1, 48.2, 48.7, 48.8
OpenVPX profile
SLT3-PAY-2F2U-14.2.3 (SOSA compatible)
Please refer to Mercury publication “Rugged Embedded Packaging and Next Generation Cooling” for specific ruggedness levels and cooling options.