EnsembleSeries™ DCM6122

Configurable, low-latency, coherent 6U OpenVPX Rx/Tx module

- **Multi-channel, highly configurable Rx/Tx Module**

- **Multi-board with internal clock generation**

- **High IBW, high analog I/O frequency, low latency**

- **Integrated FPGA processing**

The DCM6122 is a multi-channel, highly configurable Rx/Tx module with integrated FPGA processing. Optimized for demanding electronic warfare applications, it offers low-latency, high instantaneous bandwidth and high analog input/output frequency. This versatile digital transceiver is available with either front or rear I/O and is compliant to OpenVPX™ (VITA 65) to enable rapid system integration.

Coherent, Multi-board Operation

To enable modular direction finding and beam forming applications, the DCM6122 digital Rx/Tx module offers sub-sample coherency optimized to minimize the phase deviation between ports. Additionally, the product includes the hardware to enable multi-board coherency through factory-level configuration. This technology integrates clock generation and distribution hardware with proprietary phase alignment algorithms to achieve a scalable, coherent solution.

Specifications

OpenVPX Packaging

OpenVPX (VITA 65) encompasses: VITA 46.0, 46.3, 46.4, 46.6, 46.11 and VITA 48.1, 48.2 (REDI)

Data Planes

PCIe Gen 3
And/or Vita 49.2

Backplane Interface

VITA 65.0 SLT6-PAY-4F1Q2U2T-10.2.1 Slot Profile

Processor

Two Xilinx Virtex® Ultrascale+™ VU9P Prosecutors
One Ultrascale+ ZU11EG Governor
16,560 DSP Slices

Memory

16 GB DDR4 (512M x 16)
36 MB QDR4 (4M x36)

ADC

4 12-bit ADCs up to 3.2 GSPS
FS IP power across first 3 nyquist zones @2.5 GSPS: +5dBm to +15dBm, typ.

DAC

4 12-bit DACs up to 3.2 GSPS
FS OP power across first 3 nyquist zones @2.5 GSPS: -5dBm to -15dBm, typ.

FPGA Power Supplies

+0.95V @ 130A Core voltage for PRO1, PRO2, GOV
+0.85V @ 15A Core voltage for ZYNQ

Configurable Options

Front I/O or Vita 67 rear I/O

Security

System Security Engineering Ready

Other

Integrated IPMI controller
Manufactured in an AS9100D facility

Mercury Systems is a leading commercial provider of secure sensor and safety-critical processing subsystems. Optimized for customer and mission success, Mercury's solutions power a wide variety of critical defense and intelligence programs.

ACQUIRE   DIGITIZE   PROCESS   STORAGE   EXPLOIT   DISSEMINATE

Low-latency ADC/DAC Performance

Mercury's low-latency ADC/DAC products are developed to support EW applications that require real-time IF digitization and processing in harsh environments. Four 12-bit ADC channels offer individual sampling rates up to 3.2 GSPS. On the transmit side, four 12-bit, LVDS based DACs can operate up to 3.2 GSPS. Each of these DACs have convenient, user-selectable output modes to provide multi-nyquist signal projection. Optimized for EW systems, these highly configurable Rx/Tx modules deliver excellent spectral purity and efficiency, coherent multi-channel functionality and exceptional LPOI (low probably of intercept) signal detection capability. The customizable architecture can support a variety of applications including DRFM systems, beamforming, and

Advanced FPGA Functionality

Each digitized stream is passed down to Xilinx Kintex UltraScale KU115 FPGAs, each with 4GB of external DDR4 memory with an additional 18MB of QDR4 SRAM. Behind these FMC-site ingesting KU115 FPGAs lies a third Xilinx Kintex UltraScale KU115 FPGA with 8GB of external DDR4 memory along with a Xilinx Zynq UltrScale+ ZU9EG with 2GB of external DDR4 memory; offering further data processing and control prowess. The customizable architecture can support a variety of applications including DRFM systems, beamforming, and SIGINT.

Mercury's digital Rx/Tx modules are built around our EchoCore® FPGA IP to provide basic infrastructure functionality right out of the box. EchoCore IP allows customers to focus on their application while building upon the groundwork provided.

Mercury uses a simple AXI4-Stream interface for the data plane with AXI4-Stream switches for routing data within the FPGA and to external interfaces, such as PCIe. Our customers can choose their tool of choice, such as parameterizable Xilinx IPs, HLS, or RTL to generate signal processing algorithms. The cores are then instantiated into a reserved user block and compiled into the FPGAs

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Need More Help? Need a Variant of This Product?

Contact Mercury's Mixed Signal Engineering team at: digital.rf@mrcy.com or
visit www.mrcy.com/mixed-signal-processing for a detailed listing of OpenVPX products

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mercury systems®

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CORPORATE HEADQUARTERS
50 Minuteman Road
Andover, MA 01810 USA
(978) 967-1401
(866) 627-6951
Fax (978) 256-3599

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