

# 512Kx32 5V NOR FLASH MODULE

## SMD 5962-94612\*\*



WF512K32-XXX5

### FEATURES

- Access Times of 60, 70, 90, 120, 150ns
- Packaging
  - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (H2) (Package 400).
  - 68 lead, 40mm, Low Profile 3.5mm (0.140"), CQFP (Package 502)<sup>1</sup>
  - 68 lead, 22.4mm (0.880") Low Profile CQFP (G2U) 3.5mm (0.140") high, (Package 510)
  - 68 lead, 22.4mm (0.880") CQFP (G2L) 5.08mm (0.200") high, Package (528)
- 100,000 Erase/Program Cycles Minimum
- Sector Architecture
  - 8 equal size sectors of 64KBytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 512Kx32
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming

- Low Power CMOS
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Built-in Decoupling Caps for Low Noise Operation
- Page Program Operation and Internal Program Control Time
- Weight
  - WF512K32-XG2UX5 - 8 grams typical
  - WF512K32N-XH1X5 - 13 grams typical
  - WF512K32-XG4TX5<sup>(1)</sup> - 20 grams typical
  - WF512K32-XG2LX5 - 8 grams typical

\* This product is subject to change without notice.

Note 1: Package Not Recommended for New Design

For Flash programming information and waveforms refer to "Flash programming 4M5 Application Note AN0037."

\*\* For reference only. See table page 11

FIGURE 1 – PIN CONFIGURATION FOR WF512K32N-XH1X5

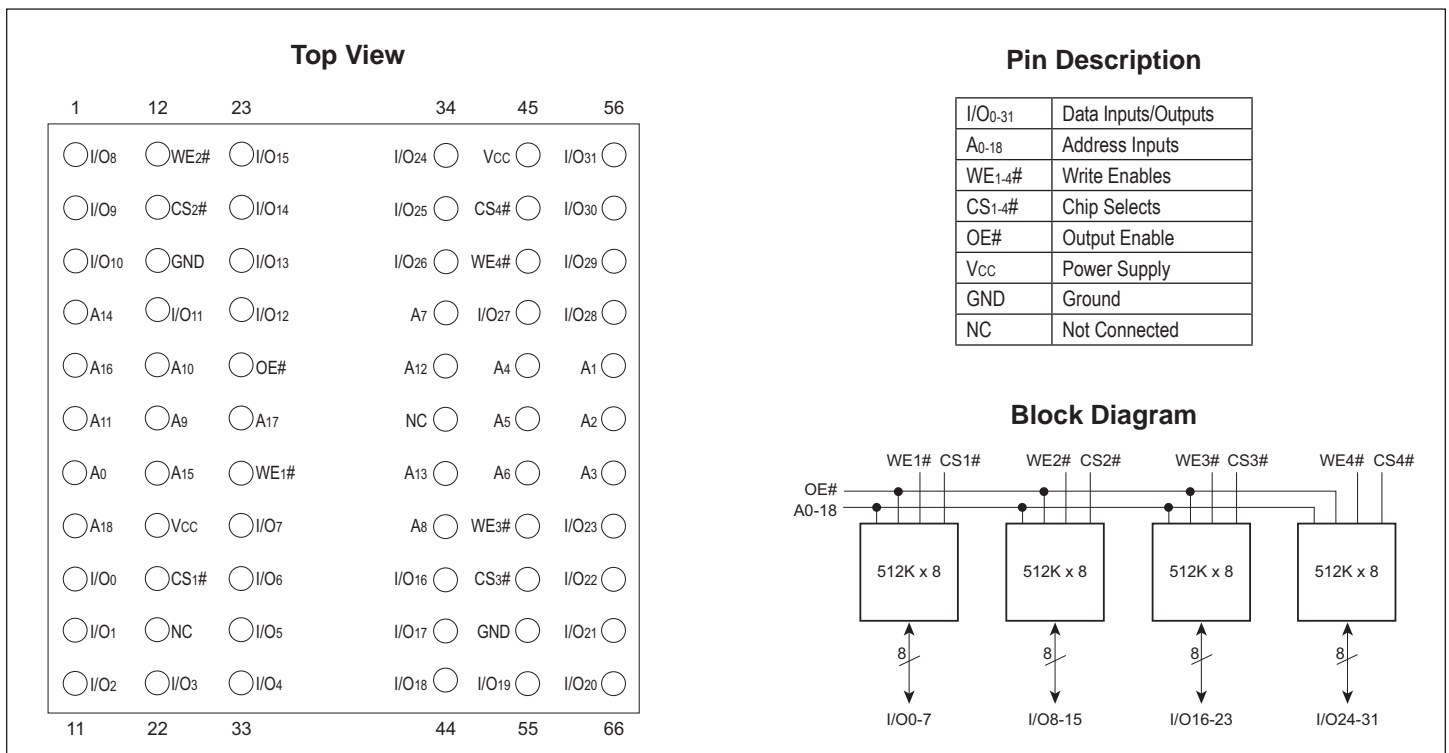


FIGURE 2 – PIN CONFIGURATION FOR WF512K32-XG4TX5<sup>1</sup>

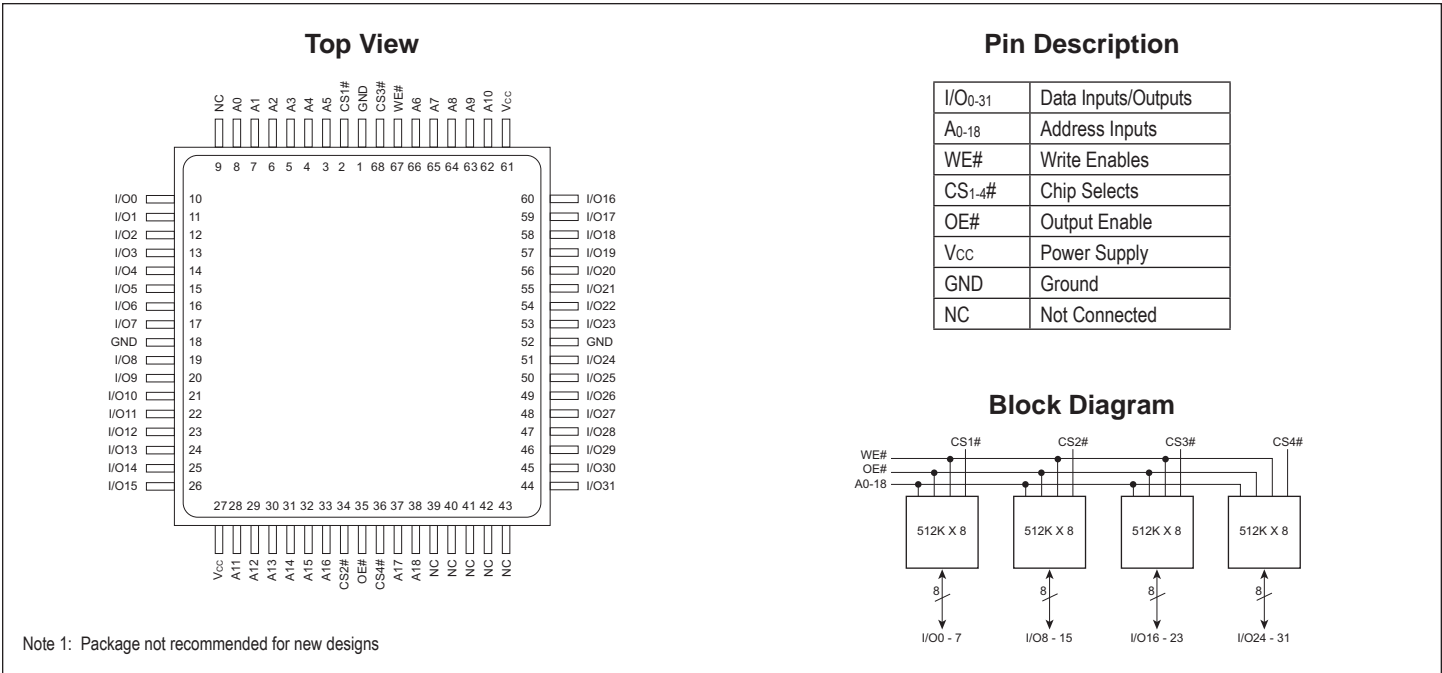
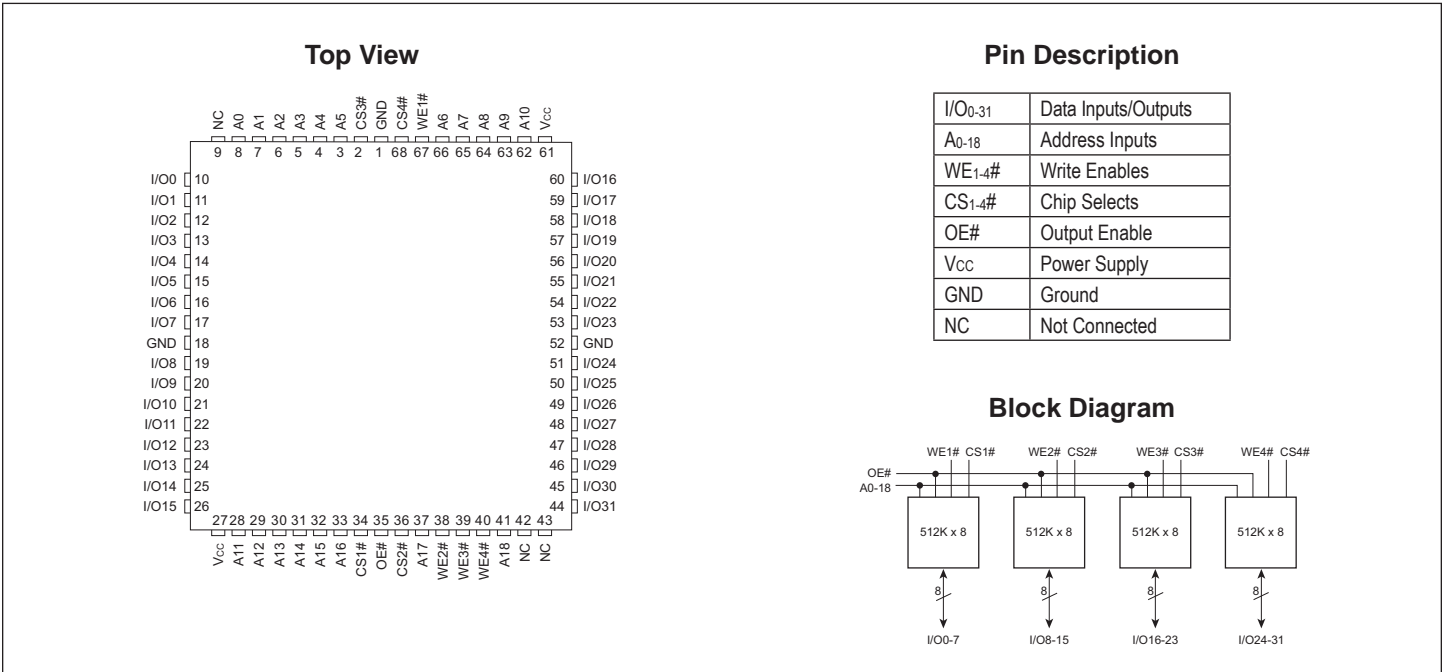


FIGURE 3 – PIN CONFIGURATION FOR WF512K32-XG2UX5 AND WF512K32-XG2LX5



**Absolute Maximum Ratings (1)**

Parameter		Unit
Operating Temperature (Mil, Q)	-55 to +125	°C
Supply Voltage Range (V <sub>CC</sub> )	-2.0 to +7.0	V
Signal voltage range (any pin except A9) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention (Mil Temp)	20 years	
Endurance - write/erase cycles	100,000 cycles min.	
A9 Voltage for sector protect (V <sub>ID</sub> ) (3)	-2.0 to +12.5	V

## NOTES:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V<sub>SS</sub> to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V<sub>CC</sub> + 0.5V. During voltage transitions, outputs may overshoot to V<sub>CC</sub> + 2.0 V for periods of up to 20ns.
- Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot V<sub>SS</sub> to -2V for periods of up to 20ns. Maximum DC input voltage on A9 is +12.5V which may overshoot to 13.5 V for periods up to 20ns.

**CAPACITANCE**T<sub>A</sub> = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	50	pF
WE1-4# capacitance HIP (PGA)	C <sub>WE</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	20	pF
CQFP G4T			50	
CQFP G2U/G2L			15	
CS1-4# capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	20	pF
Data# I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Operating Temp. (Mil., Q)	T <sub>A</sub>	-55	+125	°C
Operating Temp. (Ind.)	T <sub>A</sub>	-40	+85	°C
Operating Temp. (Com.)	T <sub>A</sub>	0	+70	°C

**DC CHARACTERISTICS**

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = V <sub>CC MAX</sub> , V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Output Leakage Current	I <sub>LOx32</sub>	V <sub>CC</sub> = V <sub>CC MAX</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	μA
V <sub>CC</sub> Active Current for Read (1, 2)	I <sub>CC1</sub>	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz		190	mA
V <sub>CC</sub> Active Current for Program or Erase (2, 3)	I <sub>CC2</sub>	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub>		240	mA
V <sub>CC</sub> Standby Current (2)	I <sub>SB</sub>	CS# = V <sub>CC</sub> ± 0.5V, f = 5MHz		6.5	mA
Input High Voltage	V <sub>IH</sub>		2.0	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>		-0.5	+0.8	V
A <sub>9</sub> Voltage for Sector Protect	V <sub>ID</sub>		11.5	12.5	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0mA, V <sub>CC</sub> = V <sub>CC MIN</sub>		0.45	V
Output High Voltage	V <sub>OHI</sub>	I <sub>OH</sub> = 2.5mA, V <sub>CC</sub> = V <sub>CC MIN</sub>	0.85 x V <sub>CC</sub>		V
Low V <sub>CC</sub> Lock-Out Voltage	V <sub>LKO</sub>		3.2	4.2	V

## NOTES:

- The I<sub>CC</sub> current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 8 mA/MHz, with OE# at V<sub>IH</sub>.
- Maximum current specifications are tested with V<sub>CC</sub> = V<sub>CC MAX</sub>
- I<sub>CC</sub> active while Embedded Algorithm (program or erase) is in progress.

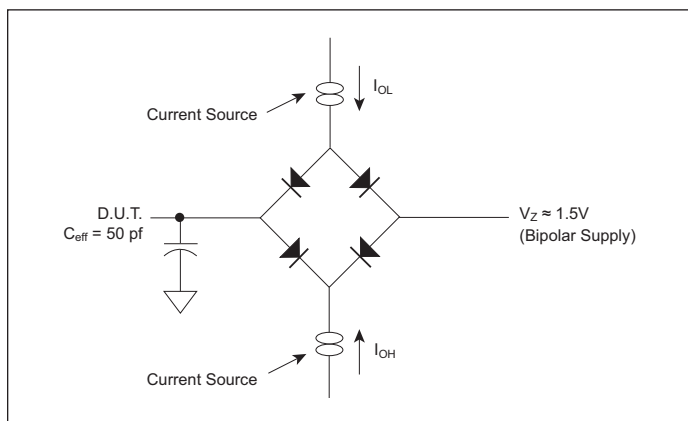
## AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, CS# CONTROLLED

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{AVAV}$	$t_{WC}$	60		70		90		120		150		ns
Write Enable Setup Time	$t_{WLEL}$	$t_{WS}$	0		0		0		0		0		ns
Chip Select Pulse Width	$t_{ELEH}$	$t_{CP}$	40		45		45		50		50		ns
Address Setup Time	$t_{AVEL}$	$t_{AS}$	0		0		0		0		0		ns
Data Setup Time	$t_{DVEH}$	$t_{DS}$	40		45		45		50		50		ns
Data Hold Time	$t_{EHDX}$	$t_{DH}$	0		0		0		0		0		ns
Address Hold Time	$t_{ELAX}$	$t_{AH}$	45		45		45		50		50		ns
Chip Select Pulse Width High	$t_{EHEL}$	$t_{CPH}$	20		20		20		20		20		ns
Duration of Byte Programming Operation (1)	$t_{WHWH1}$			300		300		300		300		300	$\mu$ s
Sector Erase Time (2)	$t_{WHWH2}$			15		15		15		15		15	sec
Read Recovery Time	$t_{GHLEL}$		0		0		0		0		0		ns
Chip Programming Time				11		11		11		11		11	sec
Chip Erase Time (3)				64		64		64		64		64	sec

## NOTES:

1. Typical value for  $t_{WHWH1}$  is 7 $\mu$ s.
2. Typical value for  $t_{WHWH2}$  is 1sec.
3. Typical value for Chip Erase Time is 8sec.

FIGURE 4 – AC TEST CIRCUIT



## AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

## Notes:

- $V_z$  is programmable from -2V to +7V.  
 $I_{OL}$  &  $I_{OH}$  programmable from 0 to 16mA.  
 Tester Impedance  $Z_0 = 75 \Omega$ .  
 $V_z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .  
 $I_{OL}$  &  $I_{OH}$  are adjusted to simulate a typical resistive load circuit.  
 ATE tester includes jig capacitance.

**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, WE# CONTROLLED**

Parameter	Symbol		Min <sup>-60</sup> Max		Min <sup>-70</sup> Max		Min <sup>-90</sup> Max		Min <sup>-120</sup> Max		Min <sup>-150</sup> Max		Unit
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	60		70		90		120		150		ns
Chip Select Setup Time	t <sub>ELWL</sub>	t <sub>CS</sub>	0		0		0		0		0		ns
Write Enable Pulse Width	t <sub>WLWH</sub>	t <sub>WP</sub>	40		45		45		50		50		ns
Address Setup Time	t <sub>AVWH</sub>	t <sub>AS</sub>	0		0		0		0		0		ns
Data Setup Time	t <sub>DVWH</sub>	t <sub>DS</sub>	40		45		45		50		50		ns
Data Hold Time	t <sub>WHDX</sub>	t <sub>DH</sub>	0		0		0		0		0		ns
Address Hold Time	t <sub>WHAX</sub>	t <sub>AH</sub>	45		45		45		50		50		ns
Write Enable Pulse Width High	t <sub>WHWL</sub>	t <sub>WPH</sub>	20		20		20		20		20		ns
Duration of Byte Programming Operation (1)	t <sub>WHWH1</sub>			300		300		300		300		300	μs
Sector Erase Time (2)	t <sub>WHWH2</sub>			15		15		15		15		15	sec
Read Recovery Time before Write	t <sub>GHWL</sub>		0		0		0		0		0		ns
VCC Set-up Time		t <sub>VCS</sub>	50		50		50		50		50		μs
Chip Programming Time				11		11		11		11		11	sec
Output Enable Setup Time		t <sub>OES</sub>	0		0		0		0		0		ns
Output Enable Hold Time (4)		t <sub>OEH</sub>	10		10		10		10		10		ns
Chip Erase Time (3)				64		64		64		64		64	sec

## NOTES:

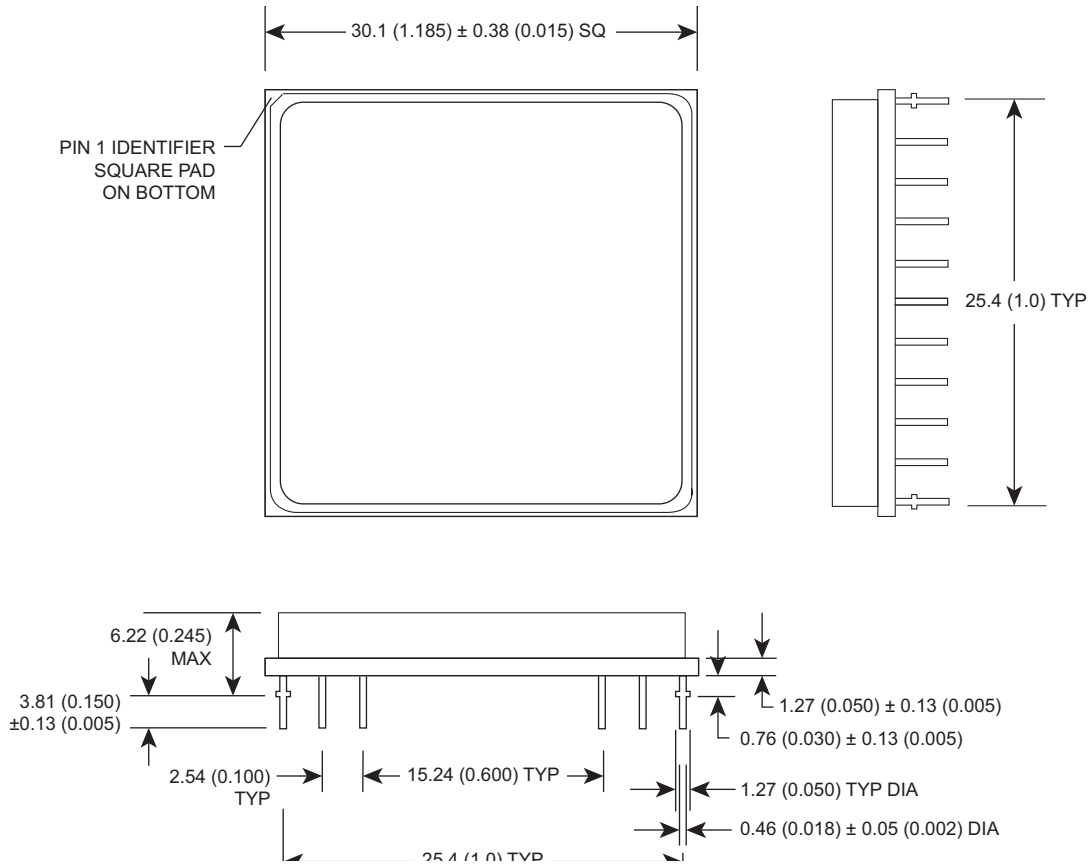
1. Typical value for t<sub>WHWH1</sub> is 7μs.
2. Typical value for t<sub>WHWH2</sub> is 1sec.
3. Typical value for Chip Erase Time is 8sec.
4. For Toggle and Data Polling.

**t<sub>AC</sub> CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, WE# CONTROLLED**

Parameter	Symbol		Min <sup>-60</sup> Max		Min <sup>-70</sup> Max		Min <sup>-90</sup> Max		Min <sup>-120</sup> Max		Min <sup>-150</sup> Max		Unit
Read Cycle Time	t <sub>AVAV</sub>	t <sub>RC</sub>	60		70		90		120		150		ns
Address Access Time	t <sub>AVQV</sub>	t <sub>ACC</sub>		60		70		90		120		150	ns
Chip Select Access Time	t <sub>ELQV</sub>	t <sub>CE</sub>		60		70		90		120		150	ns
Output Enable to Output Valid	t <sub>GLQV</sub>	t <sub>OE</sub>		30		35		35		50		55	ns
Chip Select to Output High Z (1)	t <sub>EHQZ</sub>	t <sub>DF</sub>		20		20		20		30		35	ns
Output Enable High to Output High Z (1)	t <sub>GHQZ</sub>	t <sub>DF</sub>		20		20		20		30		35	ns
Output Hold from Address, CS# or OE# Change, whichever is First	t <sub>AXQX</sub>	t <sub>OH</sub>	0		0		0		0		0		ns

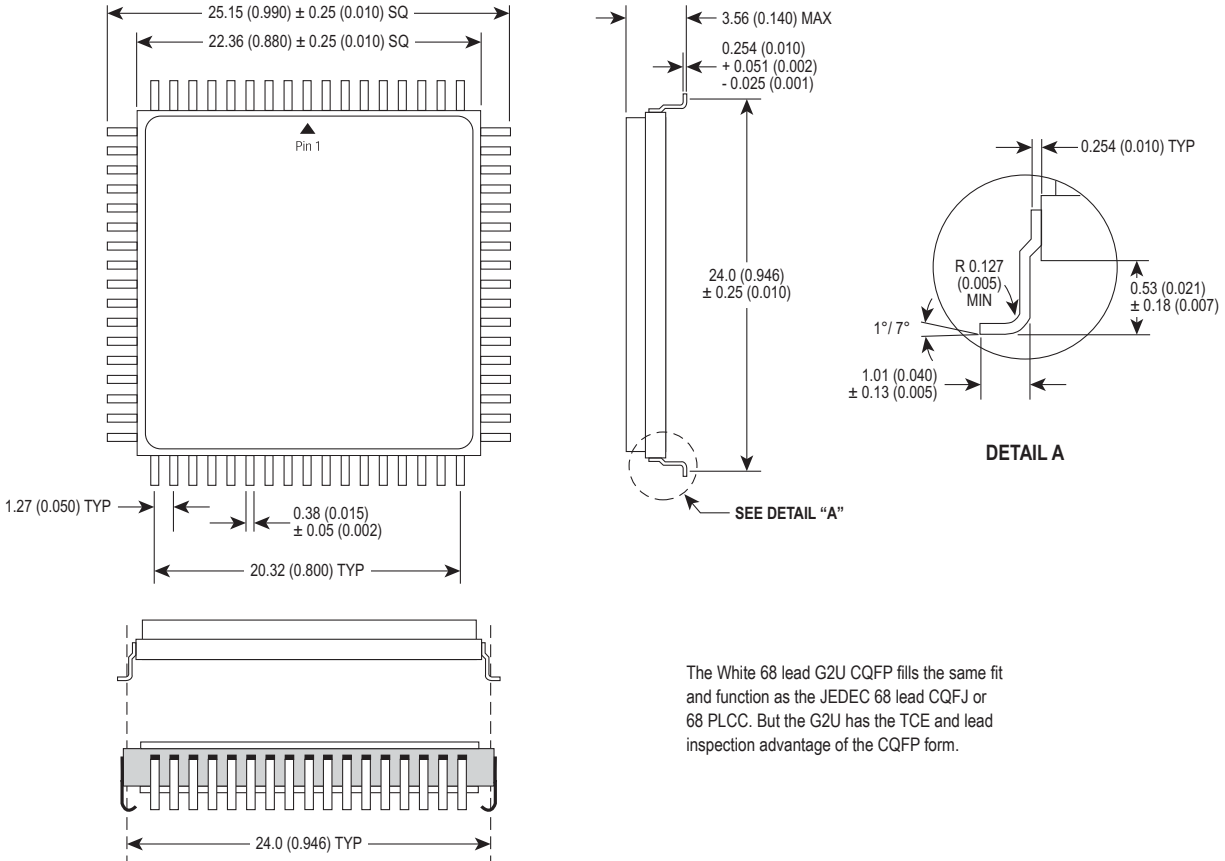
1. Guaranteed by design, but not tested

**PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

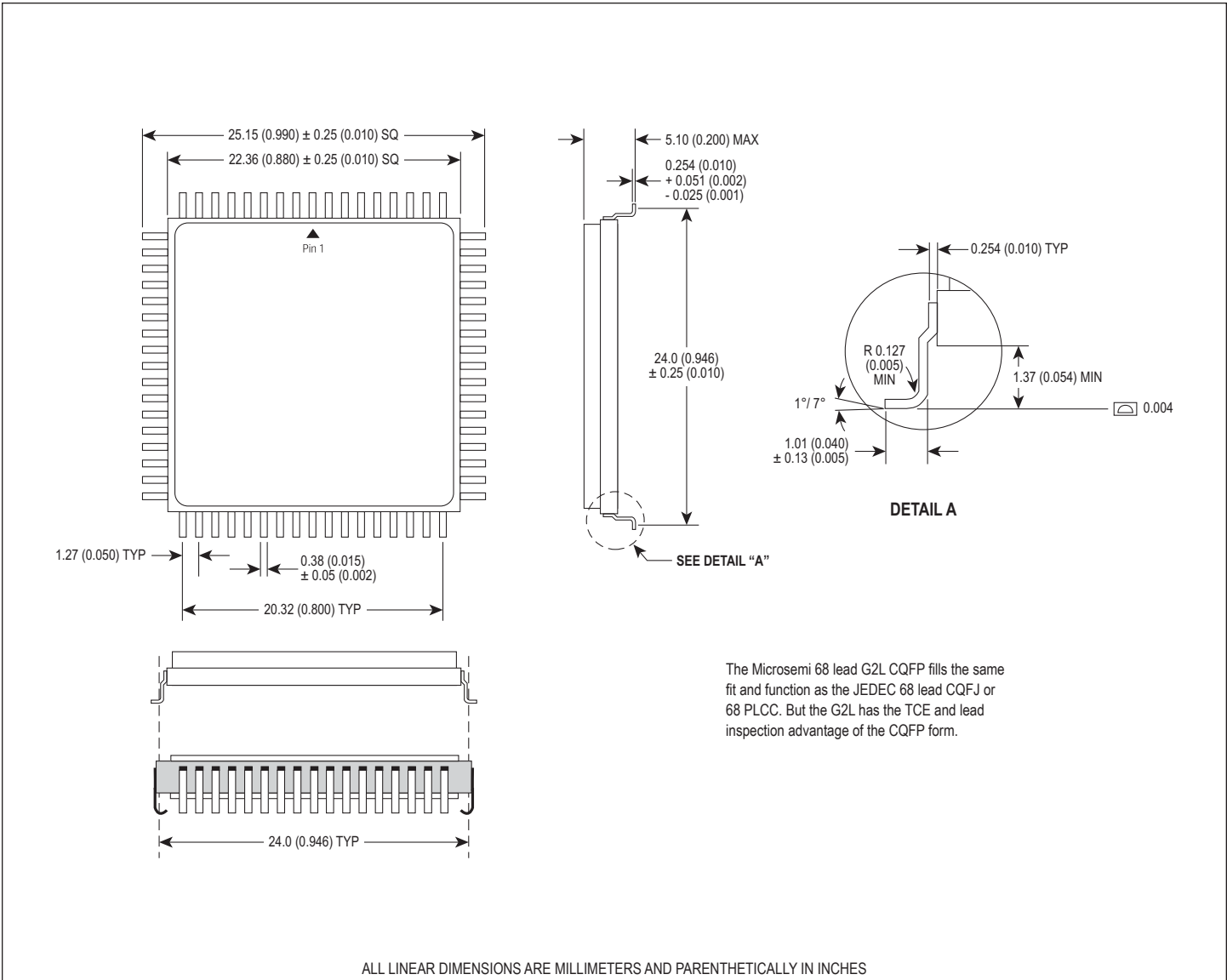
**PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)**



The White 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

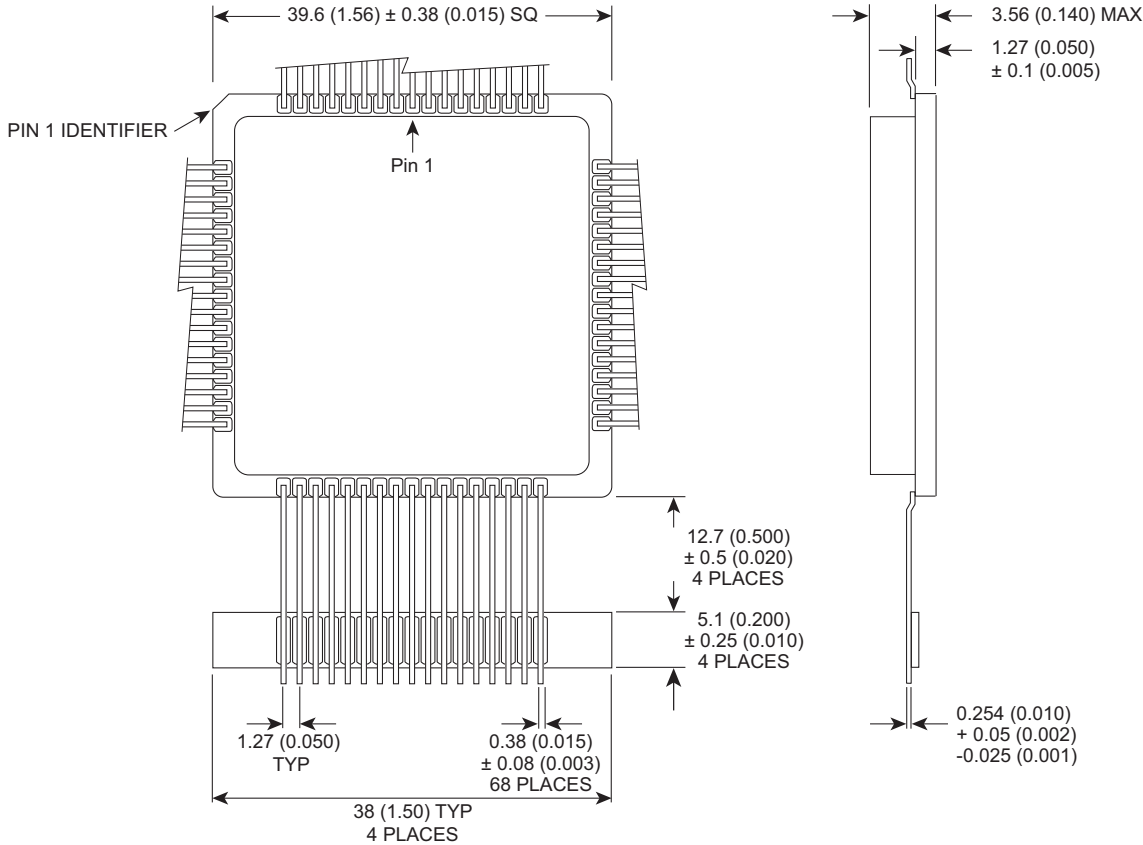
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**PACKAGE 528: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2L)**





PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)<sup>1</sup>



Note 1: Package Not Recommended for New Design

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W F 512K32 X - XXX X X 5 X

MERCURY SYSTEMS

NOR FLASH

ORGANIZATION, 512K x 32

User configurable as 1M x 16 or 2M x 8

IMPROVEMENT MARK

N = No Connect at pins 21 and 39 in HIP for Upgrade

ACCESS TIME (ns)

PACKAGE TYPE:

- H1 = 1.075" sq. Ceramic Hex In Line Package, HIP (Package 400)
- G2U = 22.4mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 510)
- G2L = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 528)
- G4T = 40mm Low Profile CQFP (Package 502)\*

DEVICE GRADE:

- Q = Military Grade\* -55°C to +125°C
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

V<sub>PP</sub> PROGRAMMING VOLTAGE

5 = 5V

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

\* Package Not Recommended for New Design  
 \*\* This product is processed the same as the 5962-XXXXXHX product but all test and mechanical requirements are per the Mercury Systems data sheet.

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 32 Flash Module	150ns	66 pin HIP (H1) 1.075" sq.	5962-94612 01H4X
512K x 32 Flash Module	120ns	66 pin HIP (H1) 1.075" sq.	5962-94612 02H4X
512K x 32 Flash Module	90ns	66 pin HIP (H1) 1.075" sq.	5962-94612 03H4X
512K x 32 Flash Module	70ns	66 pin HIP (H1) 1.075" sq.	5962-94612 04H4X
512K x 32 Flash Module	150ns	68 lead CQFP Low Profile (G4T) <sup>1</sup>	5962-94612 01HTX <sup>1</sup>
512K x 32 Flash Module	120ns	68 lead CQFP Low Profile (G4T) <sup>1</sup>	5962-94612 02HTX <sup>1</sup>
512K x 32 Flash Module	90ns	68 lead CQFP Low Profile (G4T) <sup>1</sup>	5962-94612 03HTX <sup>1</sup>
512K x 32 Flash Module	70ns	68 lead CQFP Low Profile (G4T) <sup>1</sup>	5962-94612 04HTX <sup>1</sup>
512K x 32 Flash Module	150ns	68 lead CQFP/J (G2U)	5962-94612 01HZX
512K x 32 Flash Module	120ns	68 lead CQFP/J (G2U)	5962-94612 02HZX
512K x 32 Flash Module	90ns	68 lead CQFP/J (G2U)	5962-94612 03HZX
512K x 32 Flash Module	70ns	68 lead CQFP/J (G2U)	5962-94612 04HZX
512K x 32 Flash Module	150ns	68 lead CQFP (G2L)	5962-94612 01HAX
512K x 32 Flash Module	120ns	68 lead CQFP (G2L)	5962-94612 02HAX
512K x 32 Flash Module	90ns	68 lead CQFP (G2L)	5962-94612 03HAX
512K x 32 Flash Module	70ns	68 lead CQFP (G2L)	5962-94612 04HAX

NOTE: This table is for reference only. For 5962-94612 ordering information and specifications refer to latest SMD document.

**Document Title**

512Kx32 5V NOR FLASH MODULE, SMD 5962-94612

**Revision History**

<b>Rev #</b>	<b>History</b>	<b>Release Date</b>	<b>Status</b>
Rev 13	Changes (Pg. 1-17) 13.1 Change document layout from White Electronic Designs to Microsemi 13.2 Add document Revision History page 13.3 Add "NOR" to headline	August 2011	Final
Rev 14	Changes (Pg. 1, 2, 3, 4, 13) 14.1 Delete package 501 14.2 Change 1,000,000 Erase/Program Cycles Minimum to 100,000 14.3 Change Endurance - write/erase cycles from 1,000,000 to 100,000 and A9 Voltage for sector protect from '-2.0 to + 14.0' to '-2.0 to + 12.5' in Absolute Maximum Ratings chart; change Input High Voltage Max from $V_{CC} + 0.5$ to $V_{CC} + 0.3$ , add commercial operating temp line and move $V_{IH}$ , $V_{IL}$ and $V_{ID}$ to the DC Characteristics chart; DC Characteristics – CMOS Compatible chart changes include Symbols $I_{CC4}$ to $I_{SB}$ , Conditions $V_{CC} = 5.5$ to $V_{CC} = V_{CC\ MAX}$ , $V_{IN} = GND$ to $V_{out} = GND$ , $V_{CC} = 5.5$ , $CS\# = V_{IH}$ to $CS\# = V_{CC} \pm 0.5V$ and $V_{CC} = 4.5$ to $V_{CC} = V_{CC\ MIN}$ 14.3 Change $t_{ELAX}$ -60 from 40 to 45 14.4 Change $t_{WHAX}$ -60 from 40 to 45 and $t_{OE}$ 35 to 30 14.5 Delete all Waveforms diagrams 14.6 Add NOR to Flash	May 2012	Final
Rev 15	Change (Pg. 10) 15.1 Changed Device Grade "Q" description from "MIL-STD-883 Compliant" to "MIL-PRF-38534 Class H Compliant."	May 2014	Final
Rev 16	Change (Pg. 10) 16.1 Changed Device Grade "Q" description from "MIL-PRF-38534 Class H Compliant" to "Military Grade."	August 2014	Final
Rev 17	Changes (Pg. All) (ECN 10156) 17.1 Change document layout from Microsemi to Mercury Systems	August 2016	Final