512MB (64M x 64) / 1GB (2 x 64M x 64) NOR Flash MCP 3V Page Mode Memory

W764M64V1-XBX / W7264M64V1-XBX

***ADVANCED**

FEATURES

- Single power supply operation
  - 3 Volt read, erase, and program operations
- I/O Control
  - Wide I/O voltage range (V_{IO}): 1.8V to V_{CC}
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input.
- Separate 1024-byte One Time Program (OTP) array with two lockable regions
- Uniform sector architecture
  - One thousand twenty four 128 Kbyte sectors
- 100,000 erase cycles per sector typical
- 20-year data retention typical
- Commercial, industrial and military temperature ranges
- Organized as 1 rank of 64M x 64 (512MB), 2 ranks of 64M x 64 (1GB)

PERFORMANCE CHARACTERISTICS

- High Performance
  - 110, 120 ns
  - 32-byte page read buffer
  - 15, 20 ns page read times
  - 512-byte write buffer reduces overall programming time for multiple-word updates
- Package option
  - 179 BGA, 14mm x 17mm
  - 1.0mm pitch
- Software features
  - Suspend and resume commands for program and erase operations
  - Data# polling and toggle bits provide status
  - CFI (Common Flash Interface) parameter table
- Hardware features
  - Advanced Sector Protection (ASP)
  - Hardware reset input (RESET#) resets device
  - Status Register, data polling, and ready/busy pin methods to determine device status.

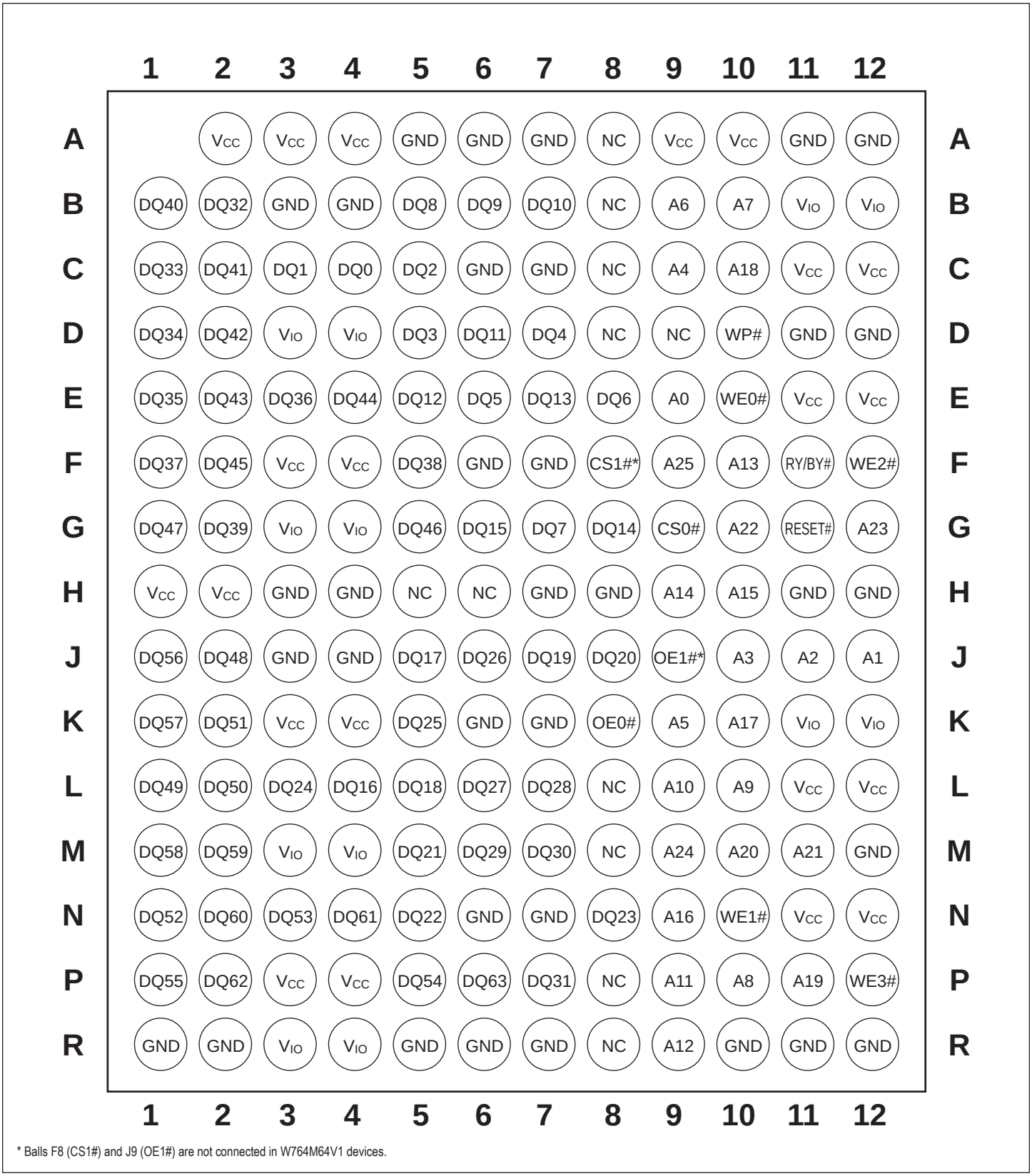
GENERAL DESCRIPTION

The W764M64V1-XBX device is a 3V single power flash memory and utilizes four chips organized as 67,108,864 words. The W7264M64V1-XBX device is a 3V single power flash memory and utilizes eight chips organized as 67,108,864 words. These devices have a 64-bit wide data bus. One write enable per 16-bit data word.

Each device requires a single 3 volt power supply for both read and write functions.

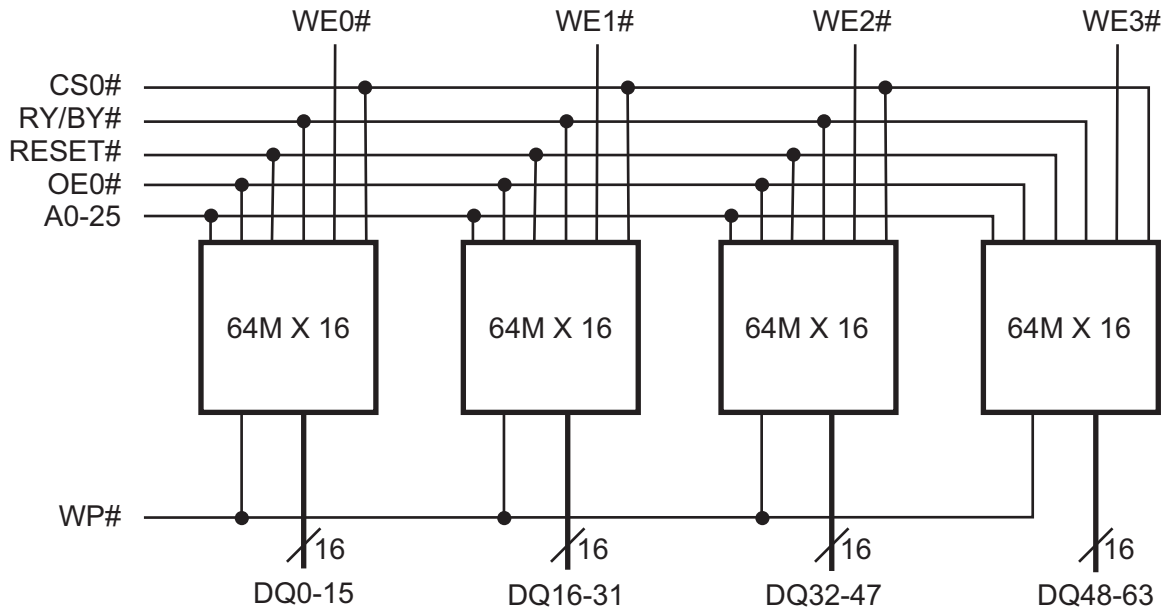
* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

FIGURE 1 – PIN CONFIGURATION (TOP VIEW)



* Balls F8 (CS1#) and J9 (OE1#) are not connected in W764M64V1 devices.

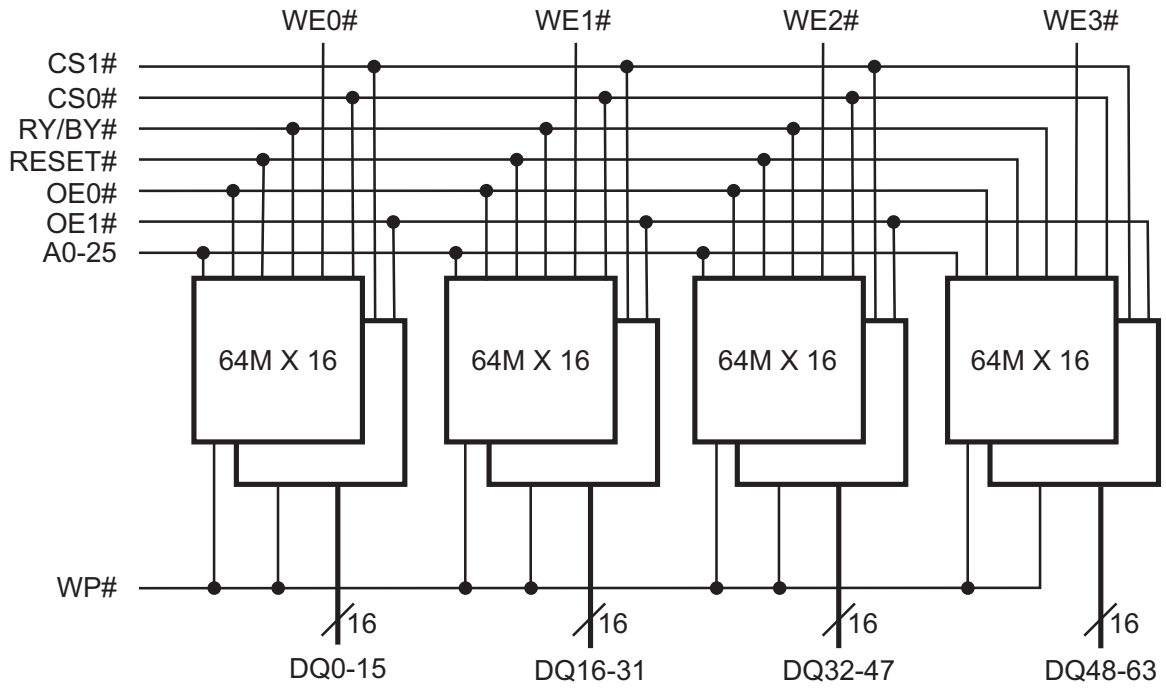
FIGURE 2 – W764M64V1 (512MB) BLOCK DIAGRAM



PIN DESCRIPTION

DQ0-63	Data Inputs/Outputs
A0-25	Address Inputs
WE0-3#	Write Enables
CS0#	Chip Select
OE0#	Output Enable
RESET#	Hardware Reset
WP#	Hardware Write Protection
RY/BY#	Ready/Busy Output
V_{CC}	Power Supply
V_{IO}	I/O Power Supply
GND	Ground
DNU	Do Not Use
NC	Not Connected

FIGURE 3 – W7264M64V1 (1GB) BLOCK DIAGRAM



PIN DESCRIPTION

DQ0-63	Data Inputs/Outputs
A0-25	Address Inputs
WE0-3#	Write Enables
CS0-1#	Chip Select
OE0-1#	Output Enable
RESET#	Hardware Reset
WP#	Hardware Write Protection
RY/BY#	Ready/Busy Output
V_{CC}	Power Supply
V_{IO}	I/O Power Supply
GND	Ground
DNU	Do Not Use
NC	Not Connected

ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Supply Voltage Range (V_{CC})	-0.5 to +4.0	V
Signal Voltage Range (other than RESET#)	-0.5 to V_{IO} +0.5	V
I/O Voltage Range (V_{IO})	-0.5 to +4.0	V
RESET#	-0.5 to V_{CC} +0.5	V
Storage Temperature Range	-55 to +125	°C

NOTES:

1. Minimum DC voltage on input or input or I/Os is -0.5V. During voltage transitions, inputs or I/Os pins may overshoot GND to -2.0V for periods of up to 20ns. Maximum DC voltage on input or I/Os pins is V_{CC} + 0.5V. During voltage transitions, input or I/O pins may overshoot to V_{CC} + 2.0V for periods up to 20ns
2. Stresses above those listed under Absolute Maxium Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of the data sheet is not implied. Exposure of the device to absolute maxium rating conditons for extended peroids may affect device reliability

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
I/O Voltage	V_{IO}	1.7	V_{CC} + 0.2	V

AC TEST CONDITIONS

Parameter	**Typ**	**Unit**
Input Pulse Levels	V_{IL} = 0, V_{IH} = V_{IO}	V
Input Rise and Fall	1.5	ns
Input and Output Reference Level	V_{IO} x 0.5	V
Output Timing Reference Level	V_{IO} x 0.5	V

NOTES:

I_{OL} & I_{OH} programmable from 0 to 16mA.

Tester Impedance Z0 = 50Ω.

V_Z is typically the midpoint of V_{OH} and V_{OL}.

I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

ATE tester includes jig capacitance.

W764M64V1 (512MB) BGA THERMAL RESISTANCE

Description	**Symbol**	**Typical**	**Units**	**Notes**
Junction to Board	Theta JB	TBD	°C/W	1
Junction to Case (Top)	Theta JC	TBD	°C/W	1

The JEDEC JESD51 specifications are used as the default modeling environment and boundary conditions. Using still air, horizontal mounting and the 2s2p board. Published material properties are used as input to derive the thermal characteristics of the module. Your application conditions will most likely differ from the JESD51 2s2p board definition specifications; therefore, Microsemi PMG recommends a customized evaluation of thermal resistances based on the actual conditions in thermally-challenged situations. Delphi models are available for most products upon request.

W7264M64V1 (1GB) BGA THERMAL RESISTANCE

Description	**Symbol**	**Typical**	**Units**	**Notes**
Junction to Board	Theta JB	TBD	°C/W	1
Junction to Case (Top)	Theta JC	TBD	°C/W	1

The JEDEC JESD51 specifications are used as the default modeling environment and boundary conditions. Using still air, horizontal mounting and the 2s2p board. Published material properties are used as input to derive the thermal characteristics of the module. Your application conditions will most likely differ from the JESD51 2s2p board definition specifications; therefore, Microsemi PMG recommends a customized evaluation of thermal resistances based on the actual conditions in thermally-challenged situations. Delphi models are available for most products upon request.

DC CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Max	Unit
Input Load Current (512MB)	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = $V_{CC(MAX)}$		±4.0	µA
Output Leakage Current (512MB)	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = $V_{CC(MAX)}$		±2.0	µA
Input Load Current (1GB)	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = $V_{CC(MAX)}$		±8.0	µA
Output Leakage Current (1GB)	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = $V_{CC(MAX)}$		±2.0	µA
V_{CC} Active Current for Read (6)	I_{CC1}	CS# = V_{IL}, OE# = V_{IH}, V_{CC} = $V_{CC(MAX)}$; address switching at 5MHz		240	mA
V_{CC} Intra-Page Read Current (6)	I_{CC2}	CS# = V_{IL}#, OE# = V_{IH}, V_{CC} = $V_{CC(MAX)}$; f = 33MHz		100	mA
V_{CC} Active Erase/Program Current (1, 6)	I_{CC3}	CS# = V_{IL}#, OE# = V_{IH}, V_{CC} = $V_{CC(MAX)}$		400	mA
V_{CC} Standby Current (6)	I_{CC4}	CS#, RESET#, OE# = V_{IH}, V_{IH} = V_{IO}, V_{IL} = V_{SS}, V_{CC} = $V_{CC\ MAX}$		400	µA
V_{CC} Reset Current (3, 5, 6)	I_{CC5}	CS# = V_{IH}, RESET# = V_{IL}, V_{CC} = $V_{CC\ MAX}$		80	mA
Automatic Sleep Mode (2, 5, 6)	I_{CC6}	V_{IH} = V_{IO}, V_{IL} = V_{SS}, V_{CC} = $V_{CC\ MAX}$, t_{ACC} + 30 ns		24	mA
		V_{IH} = V_{IO}, V_{IL} = V_{SS}, V_{CC} = $V_{CC\ max}$, t_{ASSB}		600	µA
V_{CC} current during power up (5, 6)	I_{CC7}	RESET# = V_{IO}, CS# = V_{IO}, V_{CC} = $V_{CC\ MAX}$		320	mA
Input Low Voltage	V_{IL}		-0.5	0.3 x V_{IO}	V
Input High Voltage	V_{IH}		0.7 x V_{IO}	V_{IO} + 0.4	V
Output Low Voltage (4)	V_{OL}	I_{OL} = 100 µA for DQs, I_{OL} = 2mA for RY/BY#		0.15 x V_{IO}	V
Output High Voltage	V_{OH}	I_{OH} = 100 µA	0.85 x V_{IO}		V
Low V_{CC} Lock-Out Voltage (5)	V_{LKO}		2.25	2.5	V

NOTES:

1. I_{CC} active while Embedded Algorithm is in progress.
2. Automatic sleep mode enables the lower power mode when addresses remain stable for the specified designated time.
3. If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC7} will be drawn during the remainder of t_{RPH}. After the end of t_{RPH} the device will go to standby mode until the next read or write.
4. The recommended pull-up resistor for RY/BY# output is 5k to 10k Ohms.
5. Guaranteed by design, not tested
6. Current value is for 1-rank of 64-bit data flash only.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – WE# CONTROLLED

Parameter	Symbol		-110 Min	-110 Max	-120 Min	-120 Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	60		60		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	25		25		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	30		30		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		45		ns
Write Enable Pulse Width High (3)	t_{WHWL}	t_{WPH}	20		20		ns
Single Word Programming Time (1)	t_{WHWH1}			400		400	µs
Buffer Programming Time				750		750	µs
Sector Erase (2)	t_{WHWH2}			1.1		1.1	sec
Read Recovery Time before Write (3)	t_{GHWL}		0		0		ns
Address Setup Time to OE# low during toggle bit polling		t_{ASO}	15		15		ns
Write Recovery Time from RY/BY# (3)		t_{RB}	0		0		ns
Program/Erase Valid to RY/BY# (3)		t_{BUSY}		80		80	ns

NOTES:
1. Typical value for t_{WHWH1} is 125 µs.
2. Typical value for t_{WHWH2} is 0.275 sec.
3. Guaranteed by design, not tested.

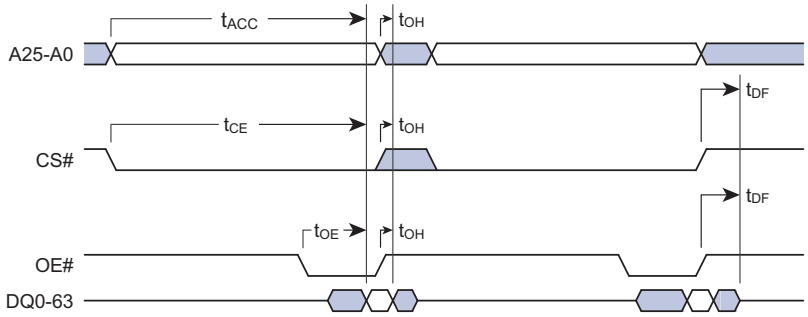
AC CHARACTERISTICS – READ-ONLY OPERATIONS

Parameter		Symbol		-110 Min	-110 Max	-120 Min	-120 Max	Unit
Read Cycle Time		t_{AVAV}	t_{RC}	110		120		ns
Address Access Time		t_{AVQV}	t_{ACC}		110		120	ns
Chip Select Access Time		t_{ELQV}	t_{CE}		110		120	ns
Page Access Time			t_{PACC}		15		20	ns
Output Enable to Output Valid		t_{GLQV}	t_{OE}		25		25	ns
Chip Select High to Output High Z		t_{EHQZ}	t_{DF}		15		15	ns
Output Enable High to Output High Z		t_{GHQZ}	t_{DF}		15		15	ns
Output Hold from Addresses, CS# or OE# Change, Whichever occurs first		t_{AXQX}	t_{OH}	0		0		ns
Output Enable Hold Time (1)	Read		t_{OEH}	0		0		ns
	Toggle and Data# Polling			10		10		ns

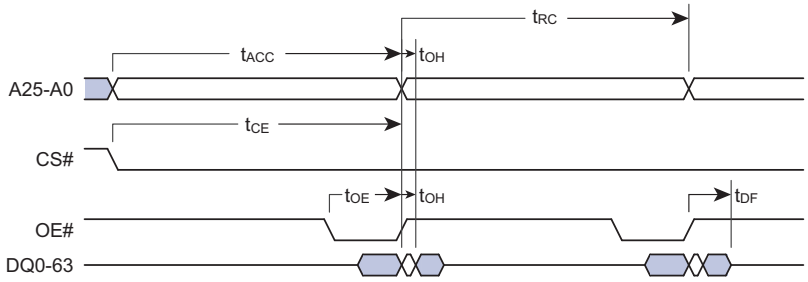
1. Guaranteed by design, not tested.

FIGURE 4 – AC WAVEFORMS FOR READ OPERATIONS

Back to Back Read (t_{ACC}) Operation Timing Diagram

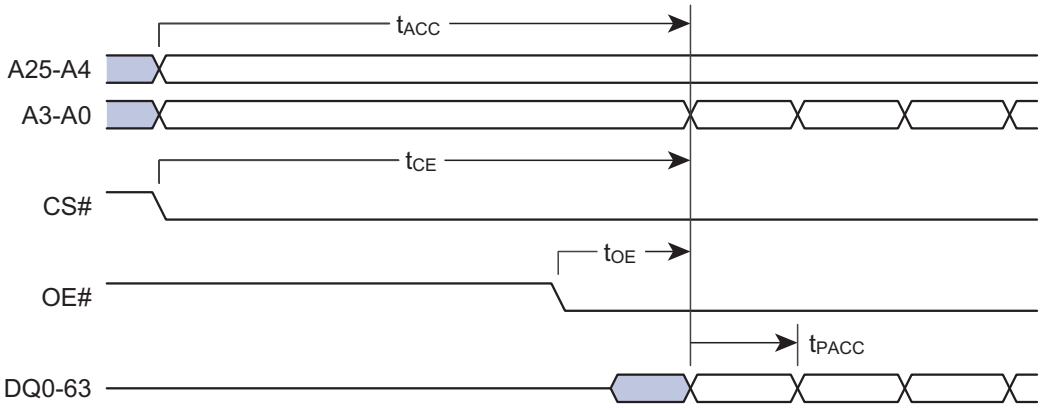


Back to Back Read Operation (t_{RC})Timing Diagram



NOTE: Back to Back operations, in which CS# remains Low between accesses, requires an address change to initiate the second access.

FIGURE 5 – PAGE READ TIMING



NOTE: Word Configuration: Toggle A0, A1, A2, and A3.

POWER ON AND RESET PARAMETERS

Parameter	Description	Limit	Value	Unit
t_{VCS}	V_{CC} Setup Time to first access (1, 2)	Min	300	µs
t_{VIOS}	V_{IO} Setup Time to first access (1, 2)	Min	300	µs
t_{RPH}	RESET# Low to CS# Low (1, 2)	Min	35	µs
t_{RP}	RESET# Pulse Width	Min	200	ns
t_{RH}	Time between RESET# (High) and CS# (low) (1)	Min	50	ns
t_{CEH}	CS# Pulse Width High (1)	Min	20	ns

NOTES:
1. Not tested.
2. Timing measured from V_{CC} reaching V_{CC} minimum and V_{IO} reaching V_{IO} minimum to V_{IH} on Reset and V_{IL} on CS#.
3. RESET# Low is optional during POR. If RESET is asserted during POR, the later of t_{RPH}, t_{VIOS}, or t_{VCS} will determine when CS# may go Low. If RESET# remains Low after t_{VIOS}, or t_{VCS} is satisfied, t_{RPH} is measured from the end of t_{VIOS}, or t_{VCS}. RESET must also be High t_{RH} before CS# goes Low.
4. $V_{CC} \geq V_{IO}$ - 200 mV during power-up.
5. V_{CC} and V_{IO} ramp rate can be non-linear.
6. Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.

FIGURE 6 – POWER-UP DIAGRAM

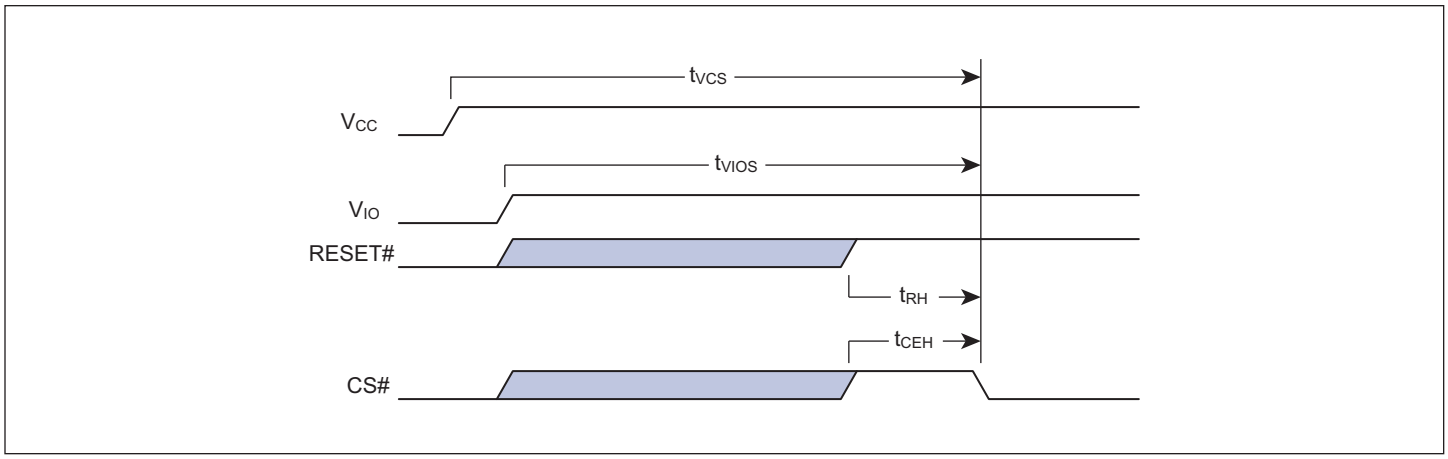


FIGURE 7 – HARDWARE RESET

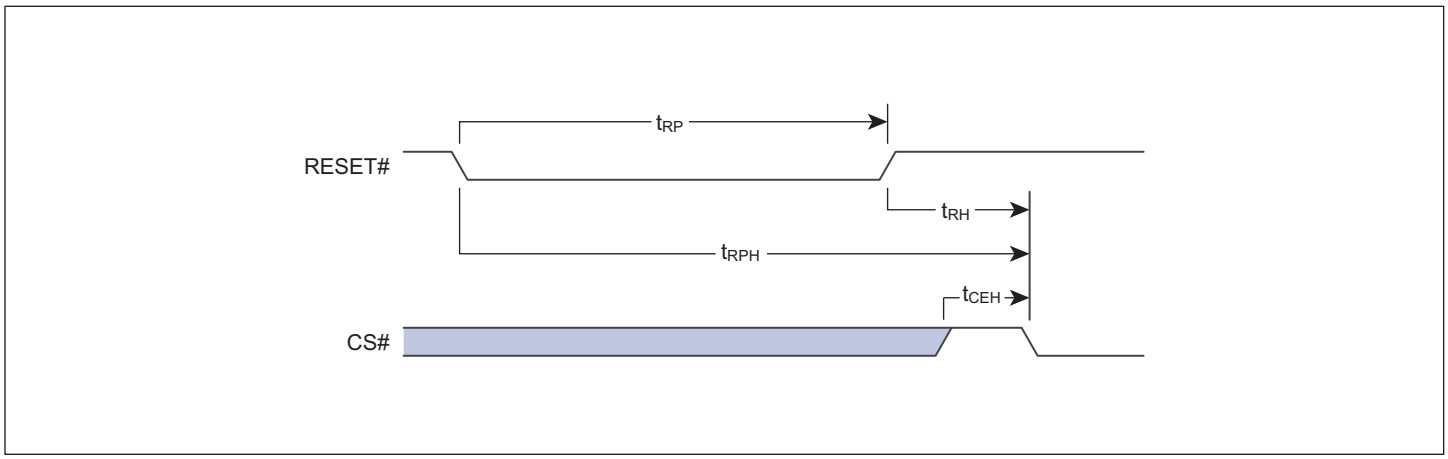


FIGURE 8 – BACK TO BACK WRITE OPERATION TIMING DIAGRAM

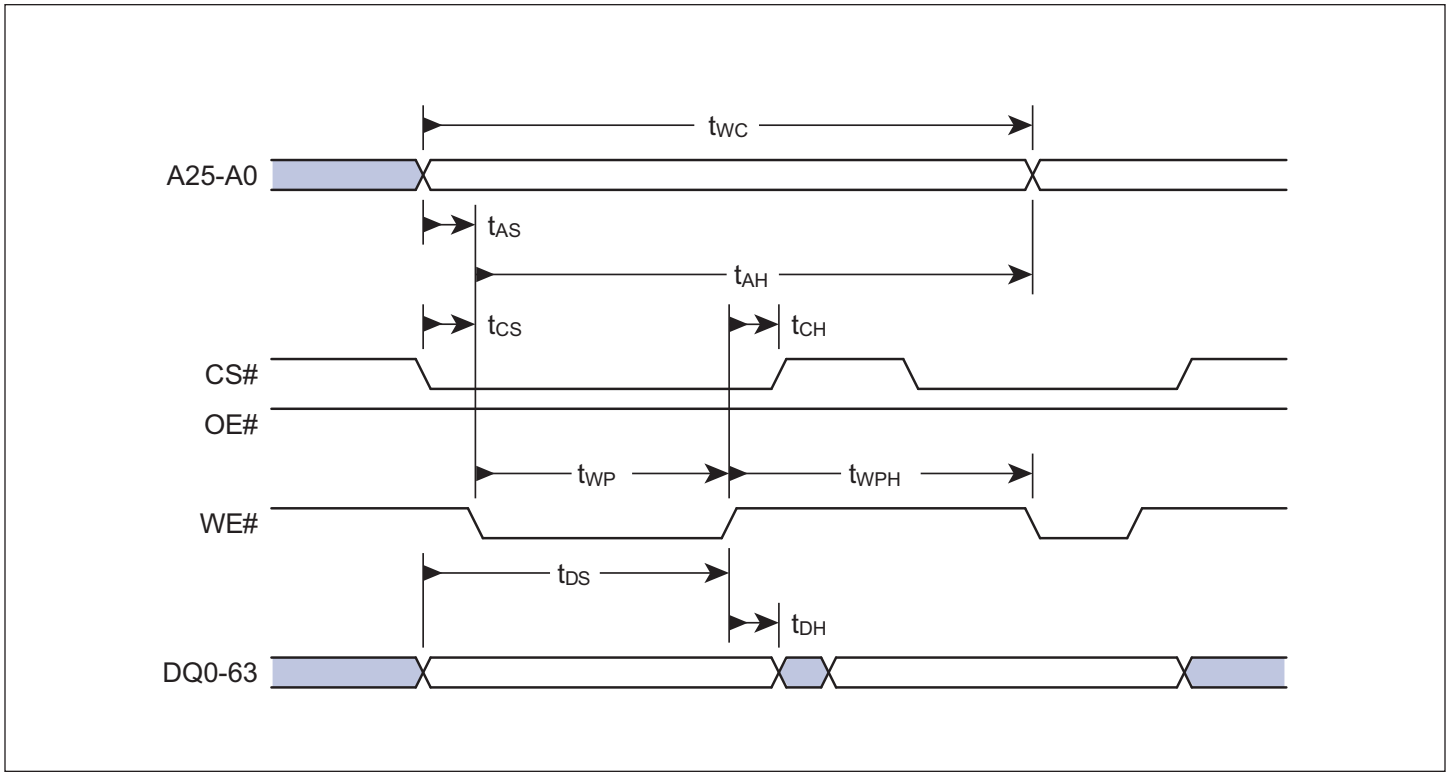


FIGURE 9 – BACK TO BACK (CS#V_{IL}) WRITE OPERATION TIMING DIAGRAM

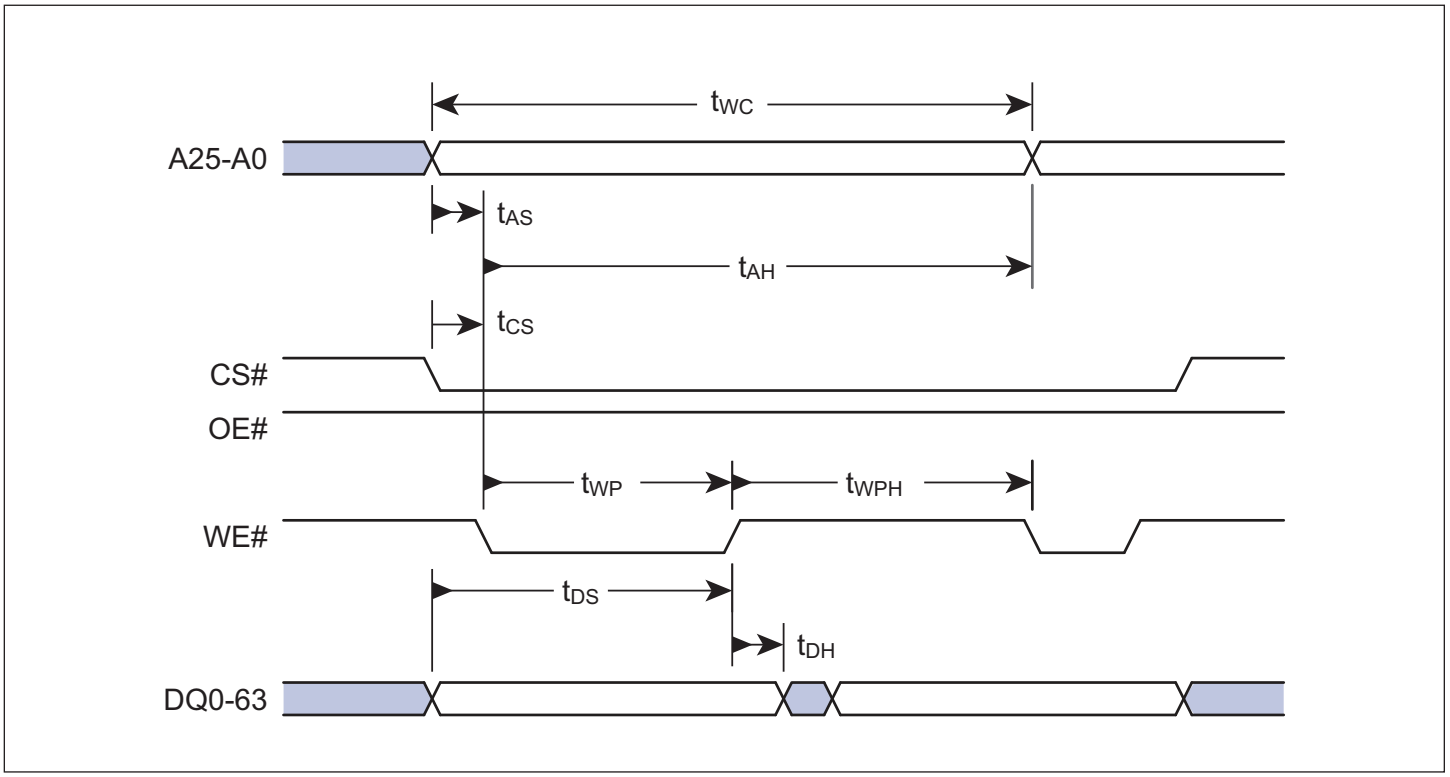


FIGURE 10 – WRITE TO READ (t_{ACC}) OPERATION TIMING DIAGRAM

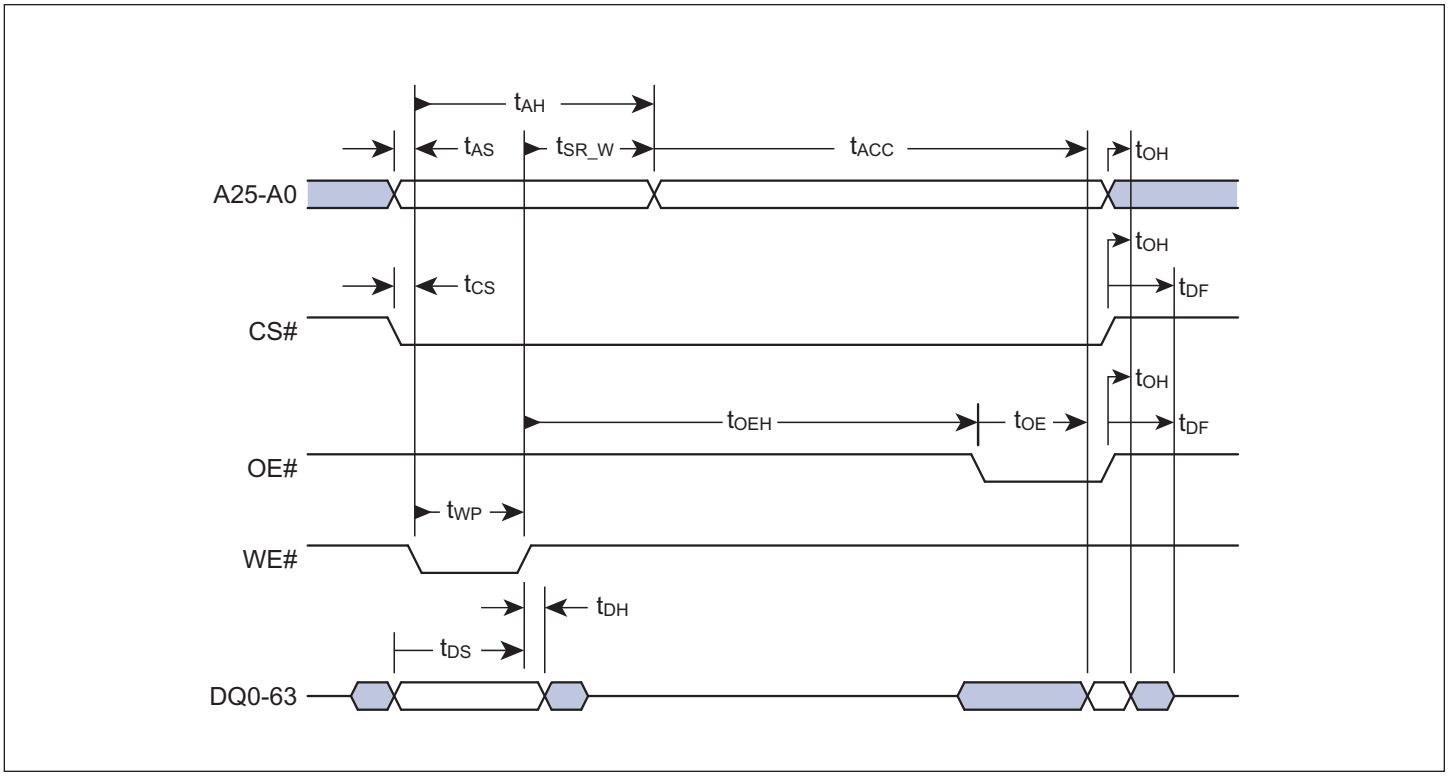


FIGURE 11 – WRITE TO READ (t_{CE}) OPERATION TIMING DIAGRAM

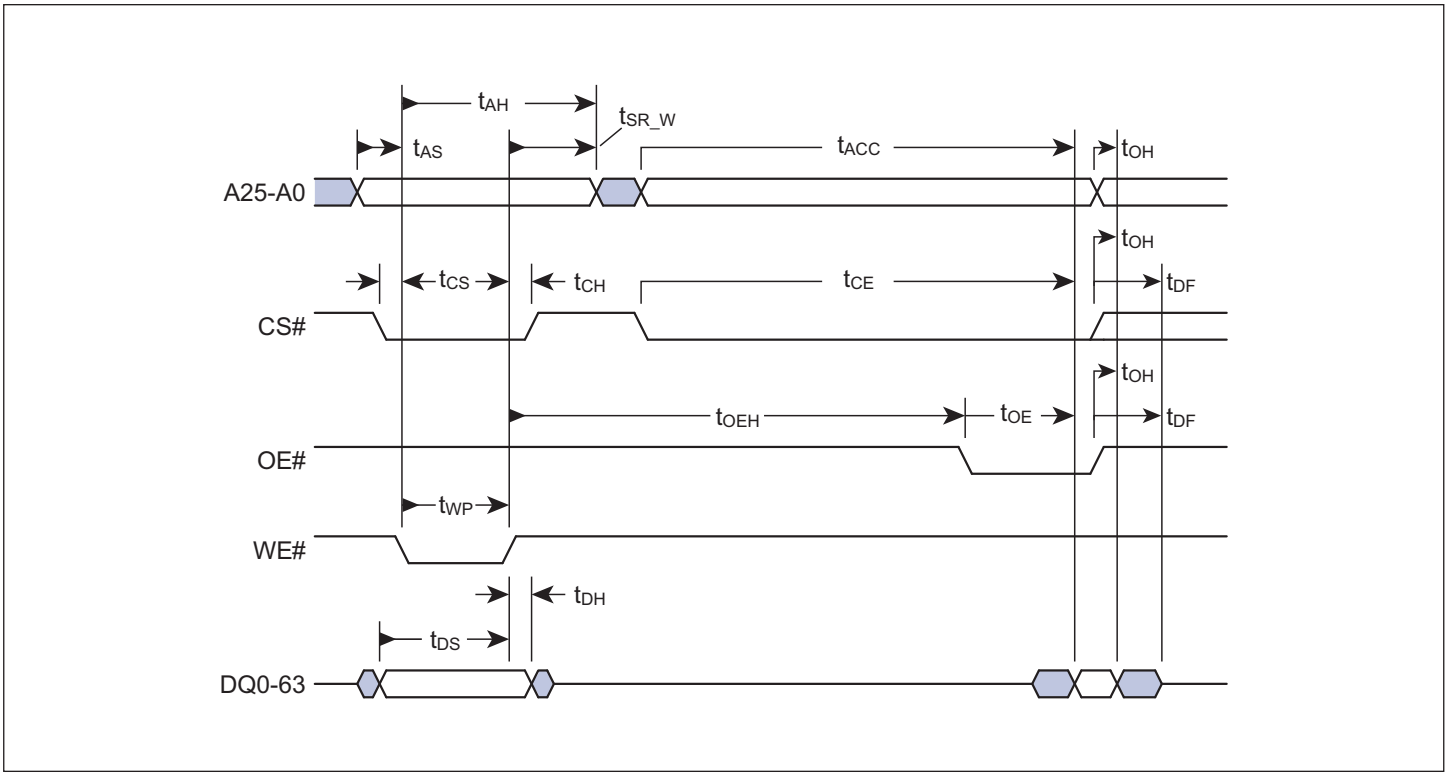


FIGURE 12 – READ TO WRITE (CS# V_{IL}) OPERATION TIMING DIAGRAM

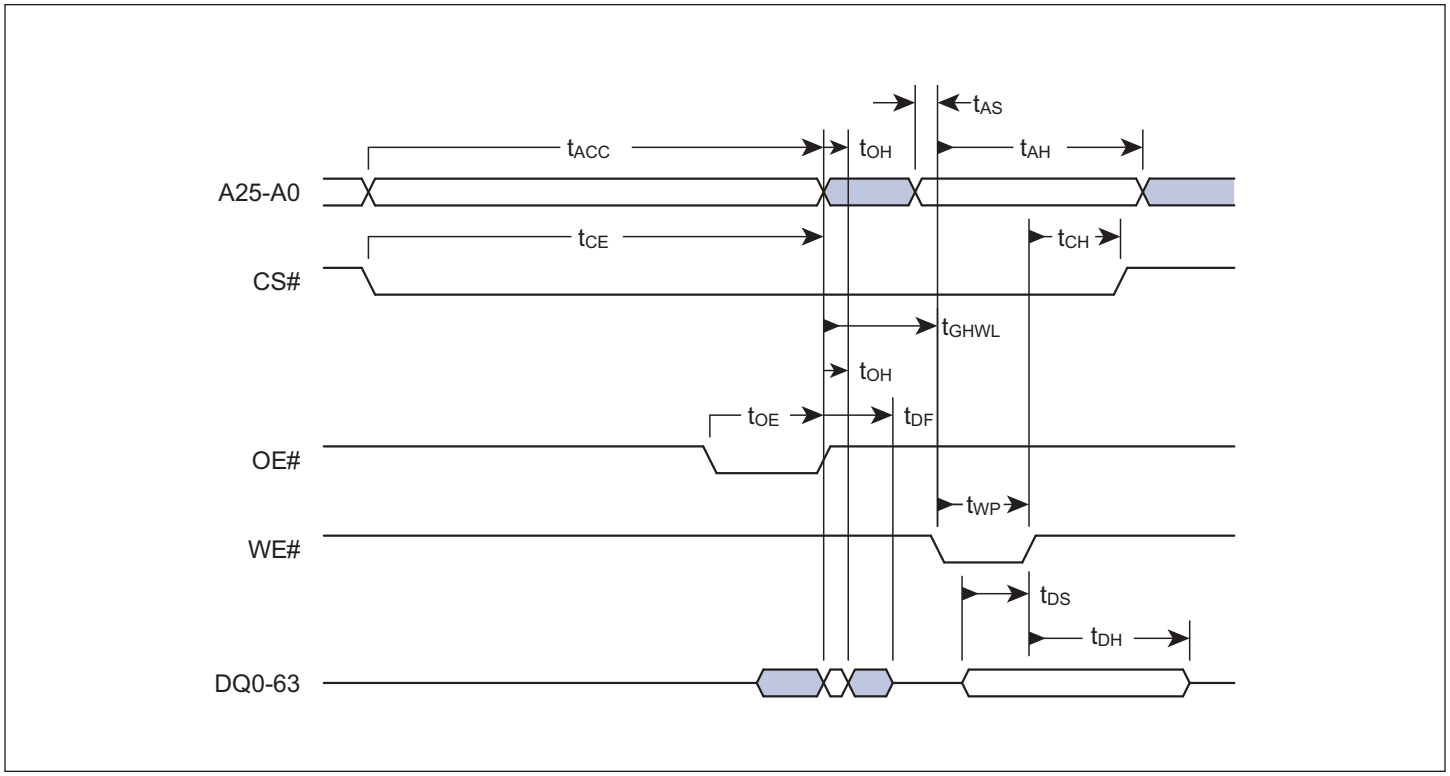


FIGURE 13 – READ TO WRITE (CS# TOGGLE) OPERATION TIMING DIAGRAM

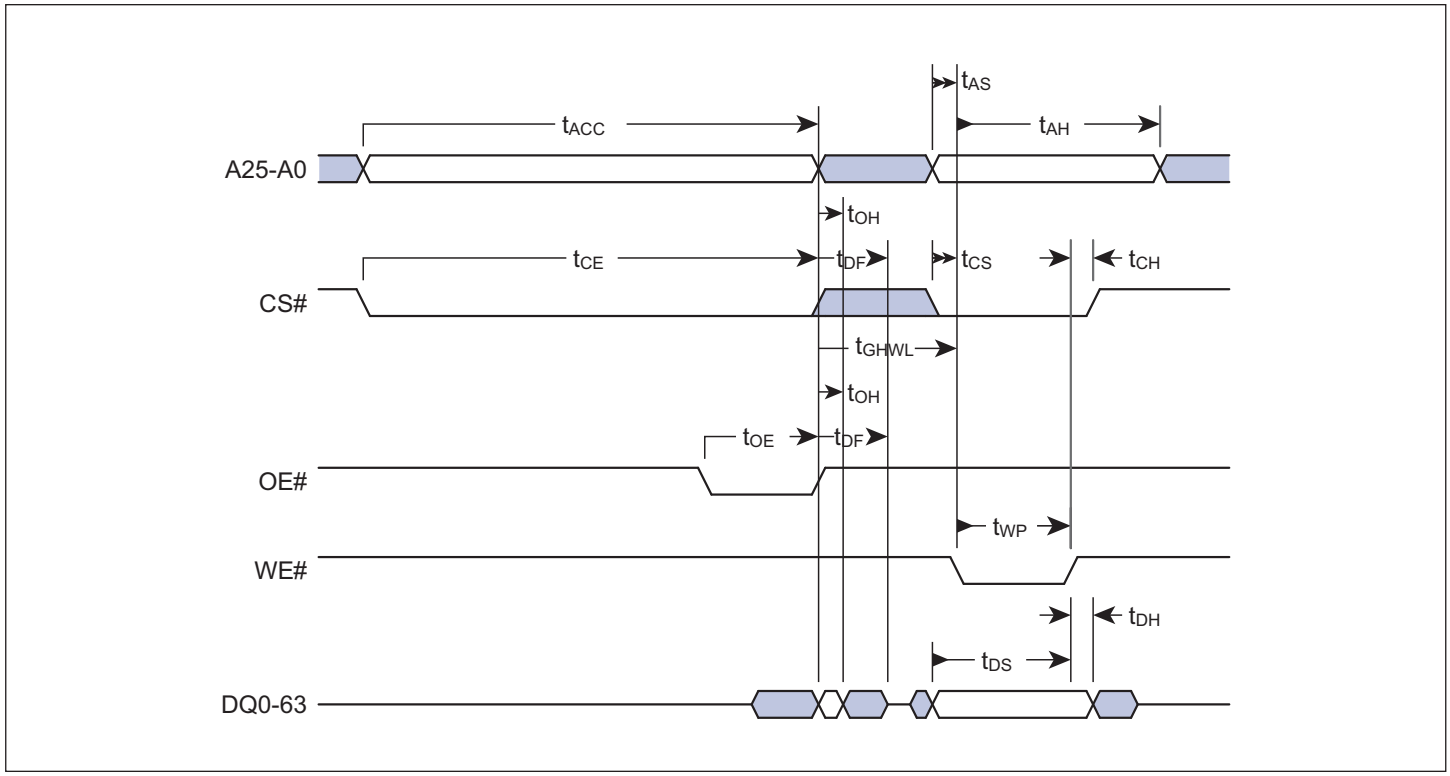
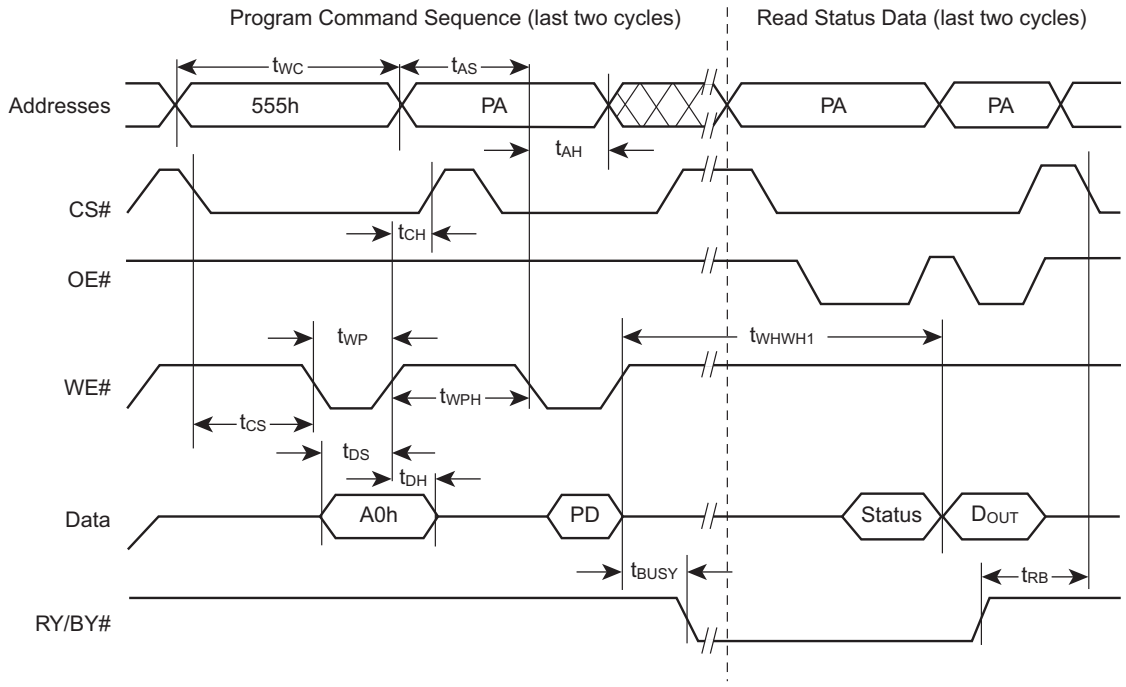
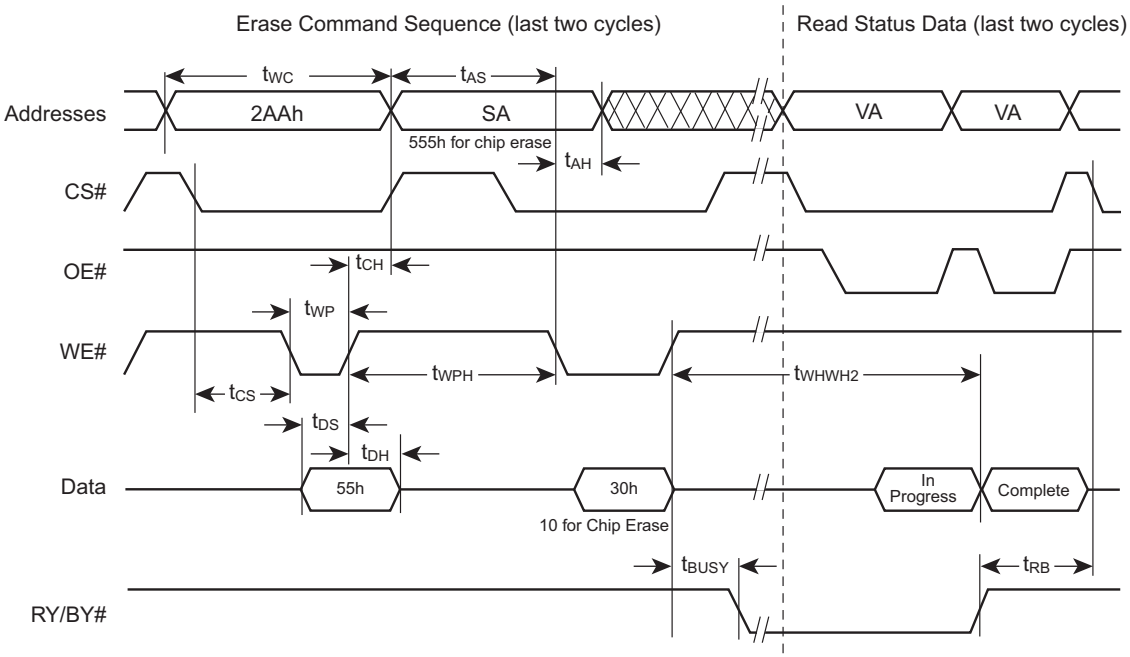


FIGURE 14 – PROGRAM OPERATIONS



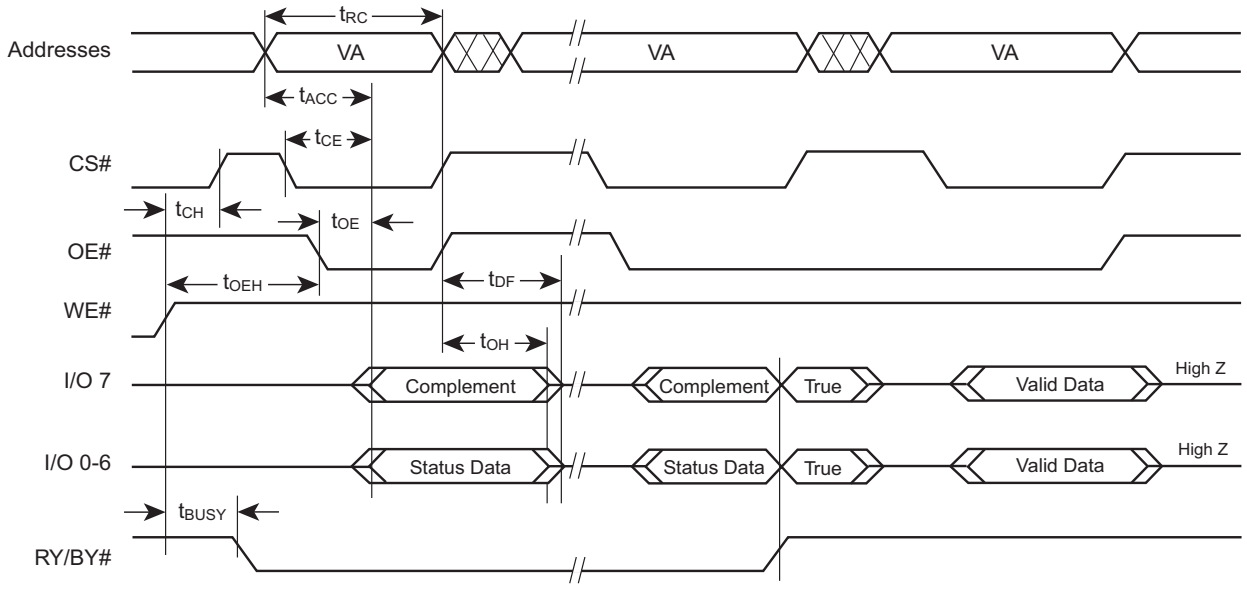
NOTE: 1. PA = program address, PD = program data, D_{OUT} is the true data at the program address.

FIGURE 15 – CHIP/SECTOR ERASE OPERATION TIMINGS



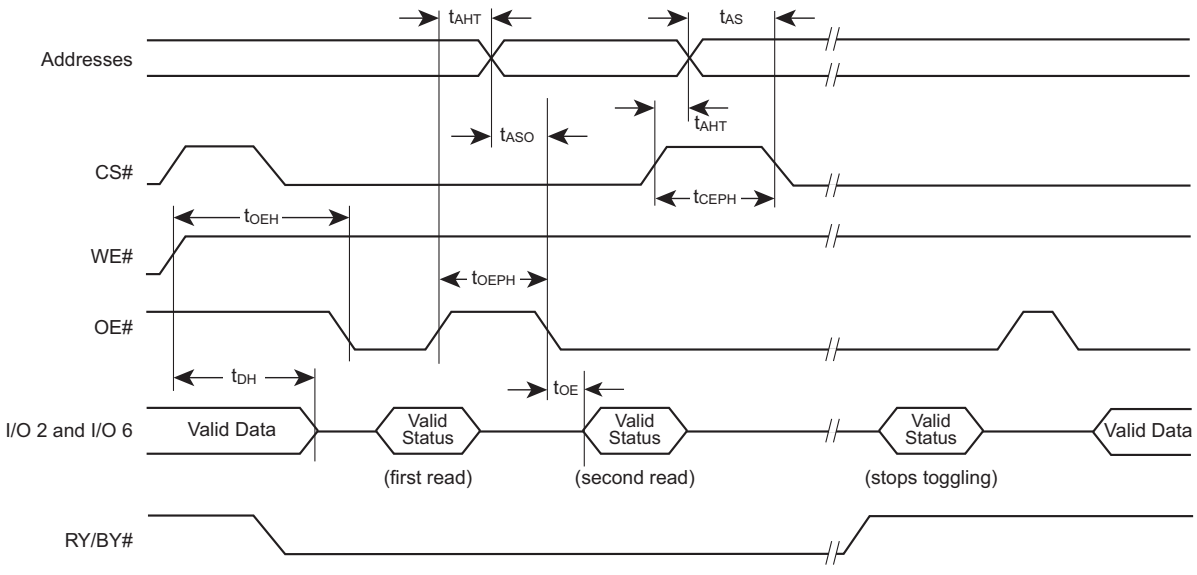
NOTE: 1. SA = Sector Address (for Sector Erase), VA = Valid Address for reading status data

FIGURE 16 – DATA POLLING TIMINGS (DURING EMBEDDED ALGORITHMS)



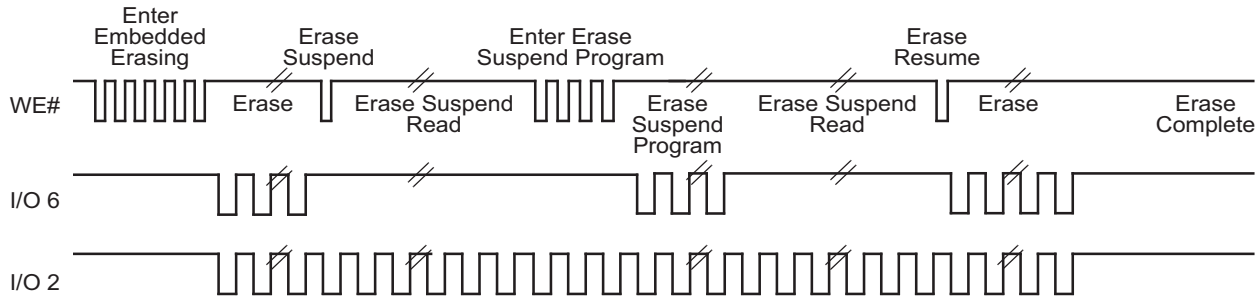
NOTE: VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

FIGURE 17 – TOGGLE BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



NOTE: 1. I/O 6 will toggle at any read address while the device is busy. I/O 2 will toggle if the address is within the actively erasing sector.

FIGURE 18 – I/O 2 Vs. I/O 6



NOTE: The system may use OE# or CS# to toggle DQ_2 and DQ_6. DQ_2 toggles only when read at an address within an erase-suspended sector.

AC CHARACTERISTICS – ALTERNATE CS# CONTROLLED ERASE AND PROGRAM OPERATIONS

Parameter				Speed Options		
JEDEC	Std	Description		110	120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	Min	60	60	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	ns
	t_{AHT}	Address Hold Time From CS# or OE# High during toggle bit polling	Min	0	0	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	30	30	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	0	ns
	t_{CEPH}	CS# High during toggle bit polling (1)	Min	20	20	ns
	t_{OEPH}	OE# High during toggle bit polling (1)	Min	20	20	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low) (1)	Min	0	0	ns
t_{WLEL}	T_{WS}	WE# Setup Time	Min	0	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0	0	ns
t_{ELEH}	t_{CP}	CS# Pulse Width	Min	25	25	ns
t_{EHEL}	t_{CPH}	CS# Pulse Width High	Min	20	20	ns
t_{WHWH1}	t_{WHWH1}	Buffer Programming Time	Typ	180	180	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Typ	0.3	0.3	sec

NOTE: 1. Not tested.

FIGURE 19 – BACK TO BACK (CS#) WRITE OPERATION TIMING DIAGRAM

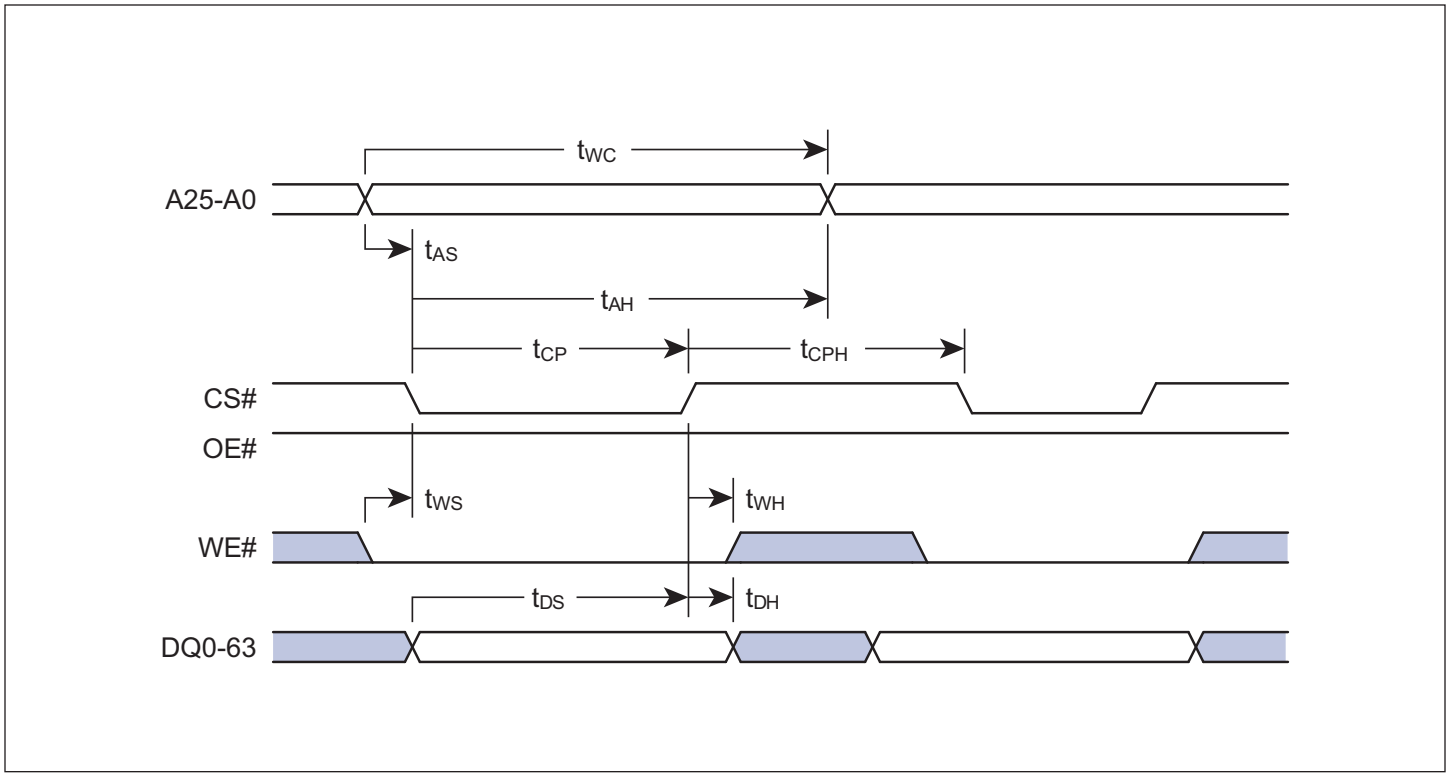
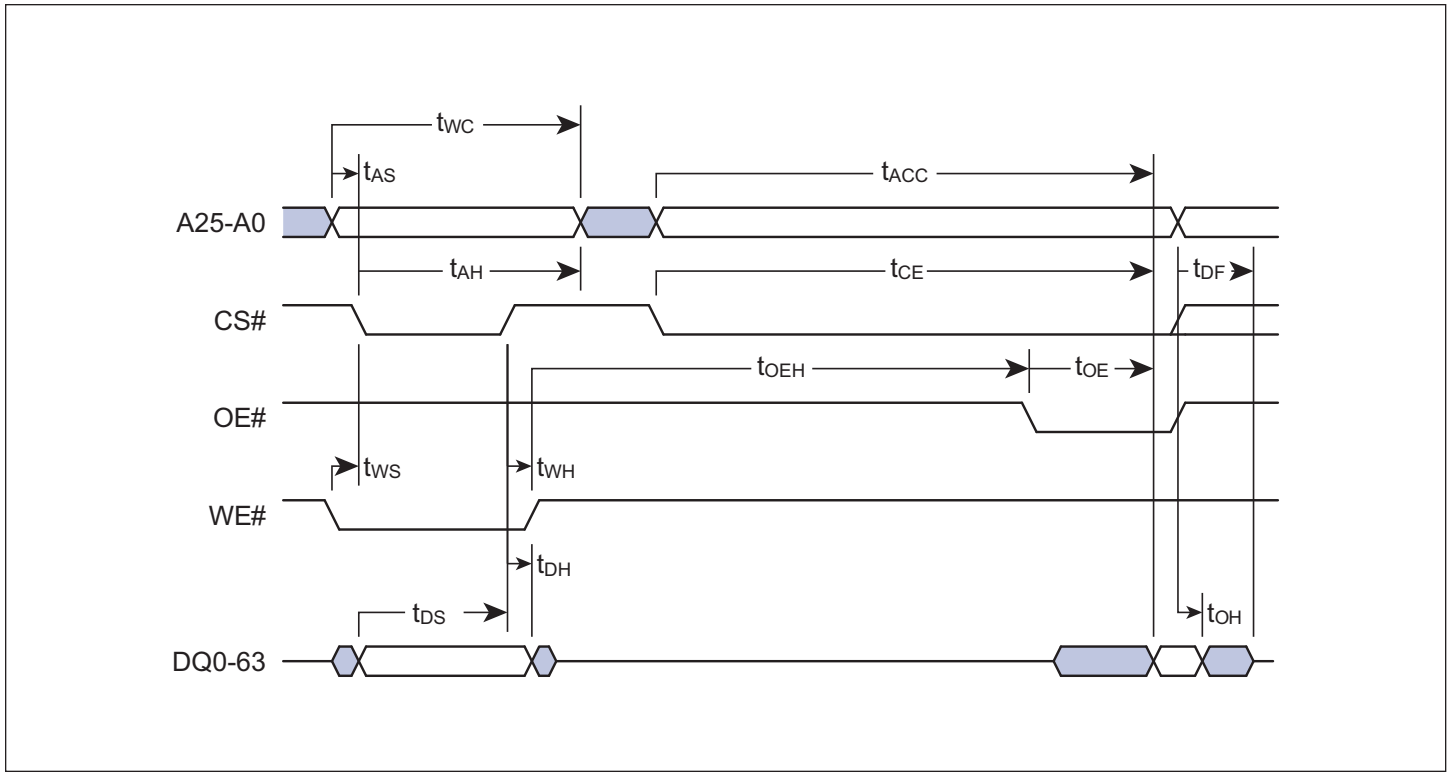
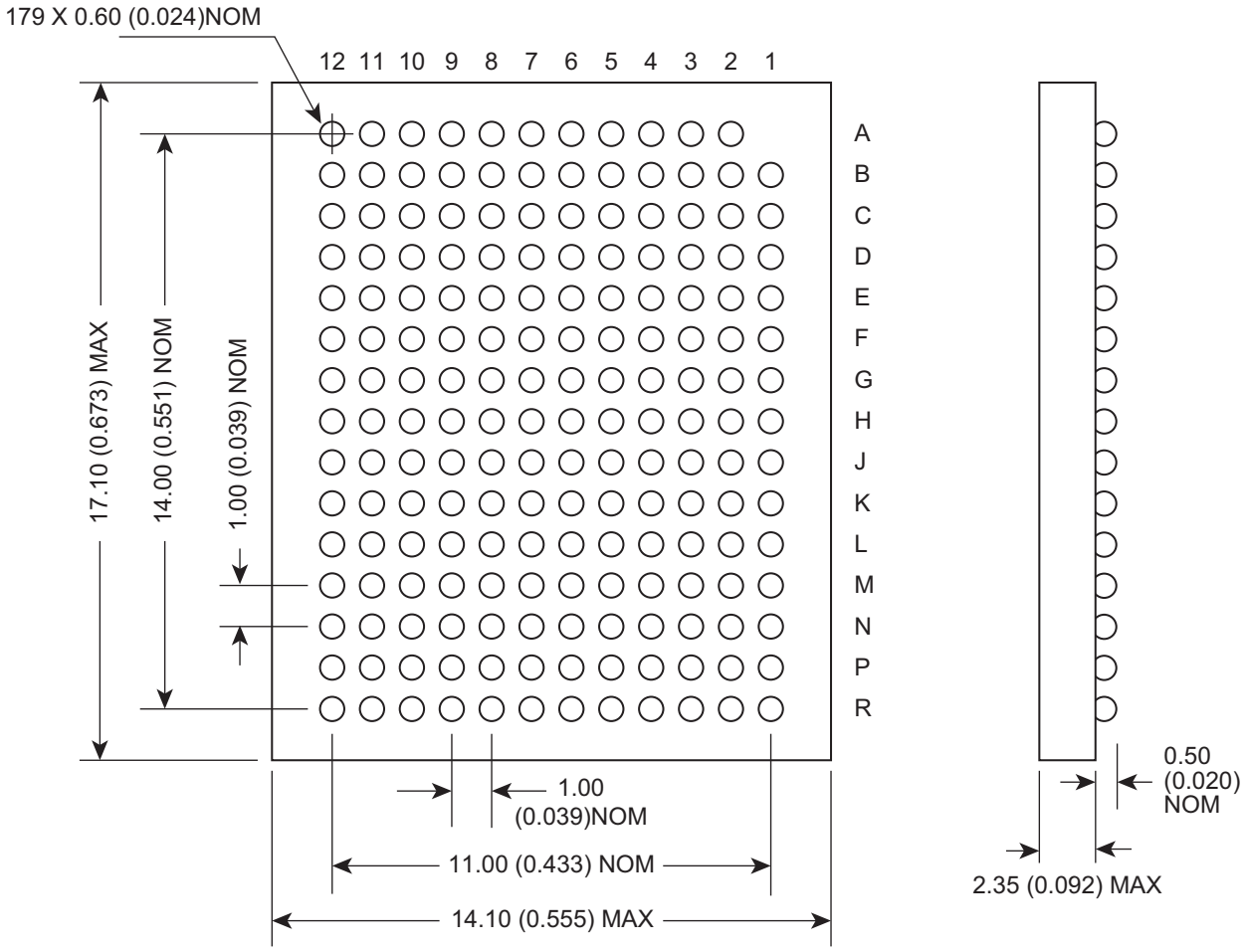


FIGURE 20 – (CS#) WRITE TO READ OPERATION TIMING DIAGRAM



W764M64V1-XBX (512MB) – 179 PBGA (PLASTIC BALL GRID ARRAY)

BOTTOM VIEW

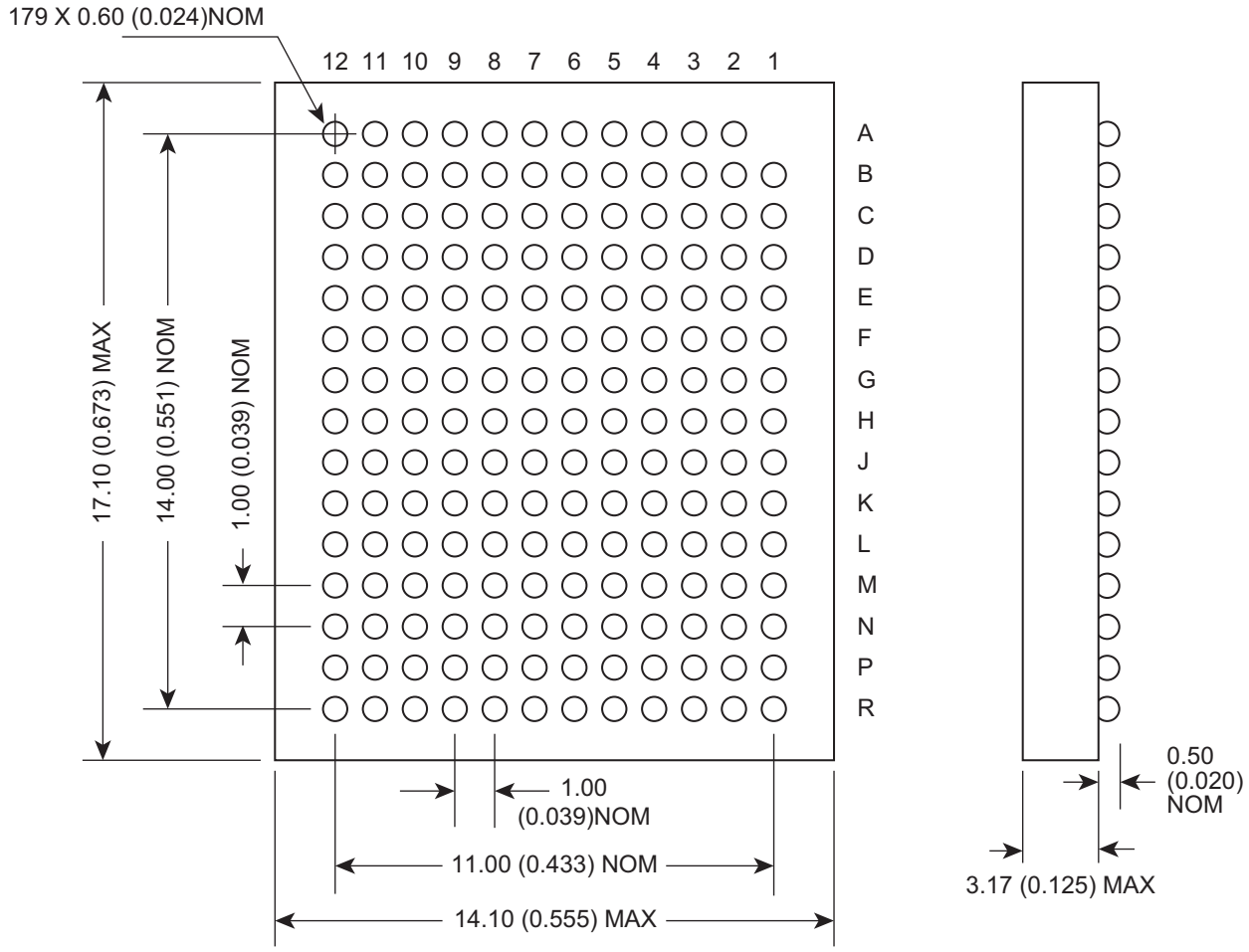


- Pads are solder mask defined, pad opening = 0.48mm

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

W7264M64V1-XBX (1GB) – 179 PBGA (PLASTIC BALL GRID ARRAY)

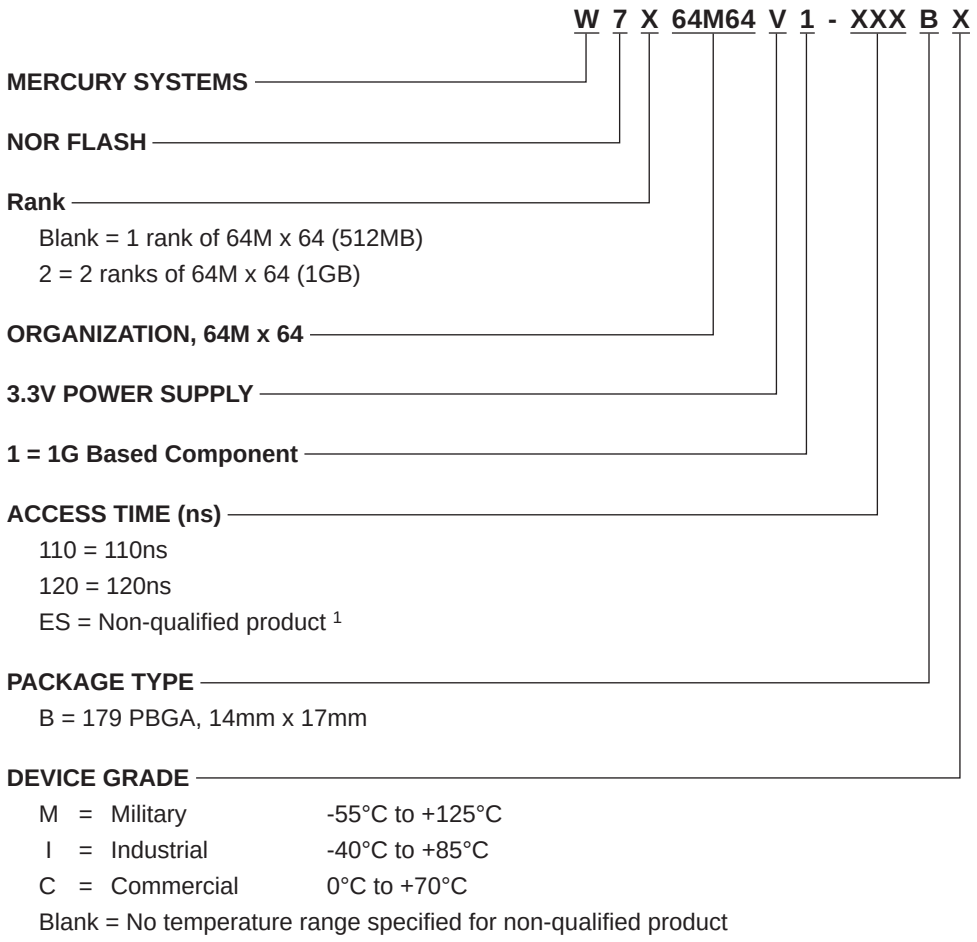
BOTTOM VIEW



- Pads are solder mask defined, pad opening = 0.48mm

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



NOTE 1: W7X64M64V1-ESB is only available product until completion of qualification.

Document Title

512MB (64M x 64) / 1GB (2 x 64M x 64) NOR Flash Multi-Chip Package 3V Page Mode Memory

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	August 2014	Advanced
Rev 1	Changes (Pg. 1-20) 1.1 Change package 153 to 179 PBGA and updated package drawings 1.2 1GB package W764M64V1-XBX_W7264M64V1-XBX change 1.3 Added pin configuration	March 2015	Advanced
Rev 2	Changes (Pg. All) (ECN 10156) 2.1 Change document layout from Microsemi to Mercury Systems	August 2016	Advanced