1Mx32 5V NOR FLASH MODULE

WEDF1M32B-XXX5

FEATURES

- Access Times of 70, 90, 120ns
- Packaging:
  - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (Package 400)
  - 68 lead, 22mm Low Profile CQFP, 3.5mm (0.140"), (Package 510)
- Sector Architecture
  - One 16KByte Sectors
  - Two 8KByte Sectors
  - One 32KByte Sectors
  - Fifteen 64KByte Sectors
- 1,000,000 Erase/Program Cycles
- Organized as 1Mx32, user configurable as 2Mx16 or 4Mx8.
- Commercial, Industrial and Military Temperature Ranges
- 5V ± 10% for Read and Write Operations.
- Low Power CMOS
- Embedded Erase and Program Algorithm
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WEDF1M32B-XG2UX5 - 8 grams typical
  WEDF1M32B-XH1X5 - 13 grams typical

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

PIN CONFIGURATION FOR WF1M32B-XH1X5

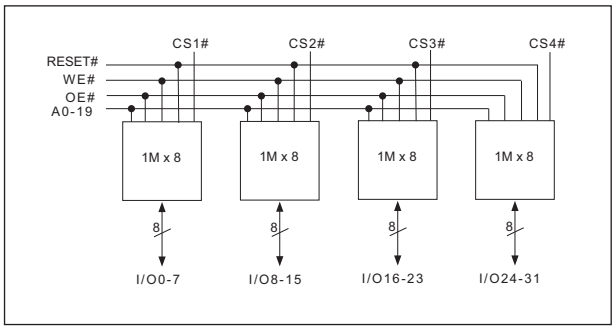
TOP VIEW

1	12	23		34	45	56
I/O8	RESET#	I/O15		I/O24	Vcc	I/O31
I/O9	CS2#	I/O14		I/O25	CS4#	I/O30
I/O10	GND	I/O13		I/O26	NC	I/O29
A14	I/O11	I/O12		A7	I/O27	I/O28
A16	A10	OE#		A12	A4	A1
A11	A9	A17		NC	A5	A2
A0	A15	WE#		A13	A6	A3
A18	Vcc	I/O7		A8	NC	I/O23
I/O0	CS1#	I/O6		I/O16	CS3#	I/O22
I/O1	A19	I/O5		I/O17	GND	I/O21
I/O2	I/O3	I/O4		I/O18	I/O19	I/O20
11	22	33		44	55	66

PIN DESCRIPTION

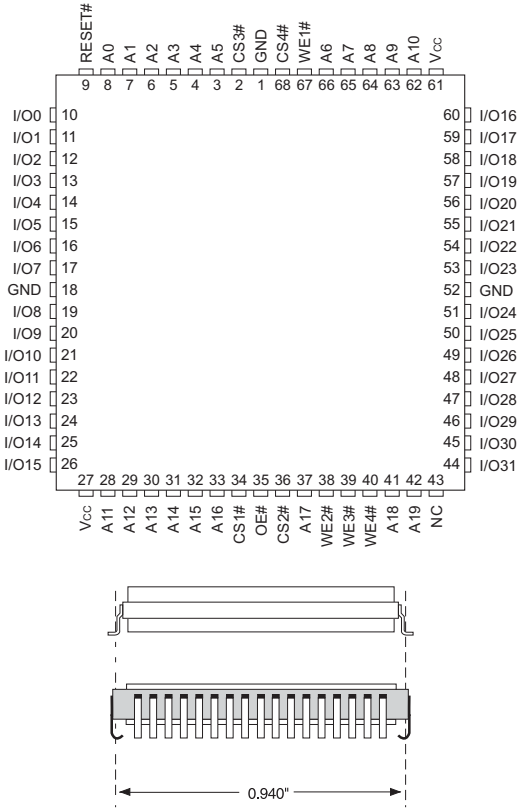
I/O0-31	Data Inputs/Outputs
A0-19	Address Inputs
WE#	Write Enable
CS1-4#	Chip Selects
OE#	Output Enable
RESET#	Reset
Vcc	Power Supply
GND	Ground
NC	Not Connected

Block Diagram



PIN CONFIGURATION FOR WF1M32B-XG2UX5

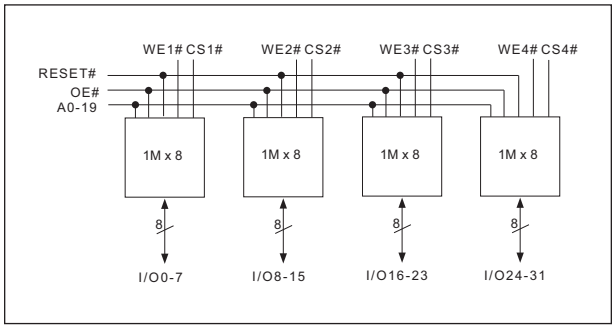
TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-19	Address Inputs
WE1-4#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
RESET#	Reset/Powerdown
V_{CC}	Power Supply
GND	Ground

BLOCK DIAGRAM



The Microsemi 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage with Respect to GND – V_{CC}	-0.5 to +7.0	V
Voltage with Respect to GND – A9, OE#, and RESET (2)	-2.0 to +12.5 V	V
Voltage with Respect to GND – All other pins (1)	-2.0 to +7.0 V	V
Output Short Circuit Current	200	mA

NOTES:
1. Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20ns.
2. Minimum DC input voltage on pins A9, OE#, and RESET is -0.5V. During voltage transitions, A9, OE#, and RESET may undershoot Vss to -2.0V for periods of up to 20ns. See Figure 6. Maximum DC input voltage on pin A9 is +12.5V which may overshoot to +13.5V for periods up to 20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a Stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

CAPACITANCE

T_A = +25°C

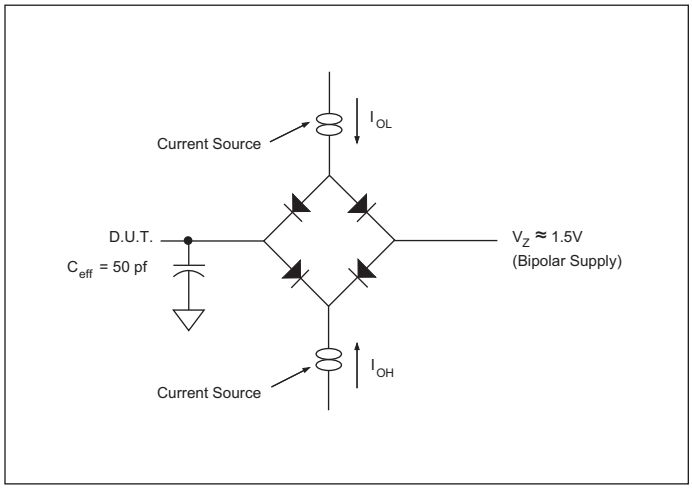
Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
WE#1-4 capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
CS1-4 capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

DC CHARACTERISTICS – CMOS COMPATIBLE

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{CC} to GND		10	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{CC} to GND		10	µA
V_{CC} Read Current (1, 2)	I_{CC1}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, IOUT = 0mA		160	mA
V_{CC} Write Current (2, 3 ,4)	I_{CC2}	CS# = V_{IL}, OE# = V_{IH}		200	mA
V_{CC} Standby Current (2, 5)	I_{CC3}	CS# = RESET# = OE# = CS = V_{IH}, f = 5MHz		20.0	µA
Output Low Voltage	V_{OL}	V_{CC} = 4.5, I_{OL} = 4.0 mA		0.45	V
Output High Voltage	V_{OH}	V_{CC} = 4.5, I_{OH} = -2.5 mA	2.4		V
Low V_{CC} Lock-Out Voltage (4)	V_{LKO}		3.2	4.2	V

NOTES:
1. The I_{CC} current listed is typically less than 2mA/MHz, with OE# at V_{IH}.
2. Maximum I_{CC} specifications are tested with V_{CC} = V_{CC} max
3. I_{CC} active while Embedded Erase or Embedded Program is in progress.
4. Not 100% tested.
5. I_{CC3} = 20µA max at extended temperature (> +85°C).

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – CS# CONTROLLED

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-70		-90		-120		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	70		90		120		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	345		45		50		ns
Address Setup Time	t_{AVWH}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	35		45		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		45		50		ns
Chip Select Hold Time	t_{WHEH}	t_{CH}	0		0		0		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		NS
Programming Operation (2)	t_{WHWH1}			300		300		300	µs
Sector Erase Operation (3)	t_{WHWH2}			8		8		8	sec
Write Recovery before Read	t_{WHECL}		0		0		0		µs
Chip Programming Time				50		50		50	sec

NOTES:
1. Guaranteed by design, not tested.
2. Typical value for t_{WHWH1} is 7µs.
3. Typical value for t_{WHWH2} is 1sec.

AC CHARACTERISTICS – WRITE OPERATIONS – CS# CONTROLLED[1]

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-70		-90		-120		Unit
			Min	Max	Min	Max	Min	Max	
Write Enable Cycle Time	t_{AVAV}	t_{WC}	70		90		120		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	35		45		50		ns
Address Setup Time	t_{AVEH}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	30		45		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{EHAX}	t_{AH}	45		45		50		ns
Write Enable Hold Time	t_{EHWH}	t_{WH}	0		0		0		ns
Chip Select Pulse Width High	t_{EHEL}	t_{EPH}	20		20		20		µs
Programming Operation (1)	t_{WHWH1}			300		300		300	sec
Sector Erase Operation (2)	t_{WHWH2}			8		8		8	µs
Write Recovery before Read	t_{EHGL}		0		0		0		µs

NOTES:
1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 1sec.

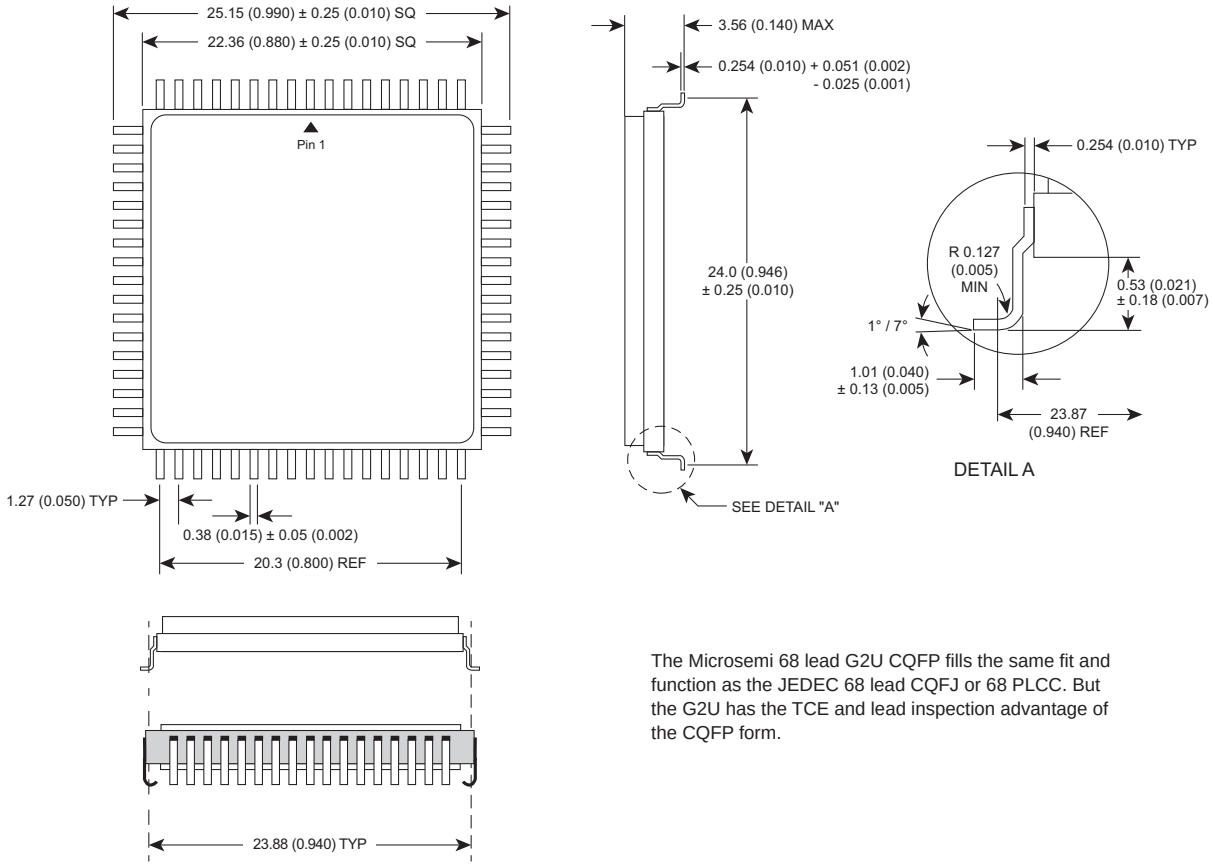
AC CHARACTERISTICS – READ-ONLY OPERATIONS

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-70		-90		-120		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	70		90		120		ns
Address Access Time	t_{AVQV}	t_{ACC}		70		90		120	ns
Chip Select to Output Valid (1)	t_{ELQV}	t_{CE}		70		90		120	ns
Output Enable to Output Valid (1)	t_{GLQV}	t_{OE}		30		35		50	ns
Chip Select to Output Low Z (2)	t_{ELQX}	t_{LZ}	0		0		0		ns
Chip Select High to Output High Z (2)	t_{EHQZ}	t_{HZ}		20		20		50	ns
Output Enable to Output Low Z (2)	t_{GLQX}	t_{OLZ}	0		0		0		ns
Output Enable High to Output High Z (2)	t_{GHQZ}	t_{DF}		20		20		30	ns
Output Hold from Addresses, CS# or OE# Change, Whichever is First (2)		t_{OH}	0		0		0		ns

NOTES:
1. OE# may be delayed up to t_{CE}-t_{OE} after the falling edge of CS# without impact on t_{CS}.
2. Guaranteed by design, not tested.

PACKAGE 510 – 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)



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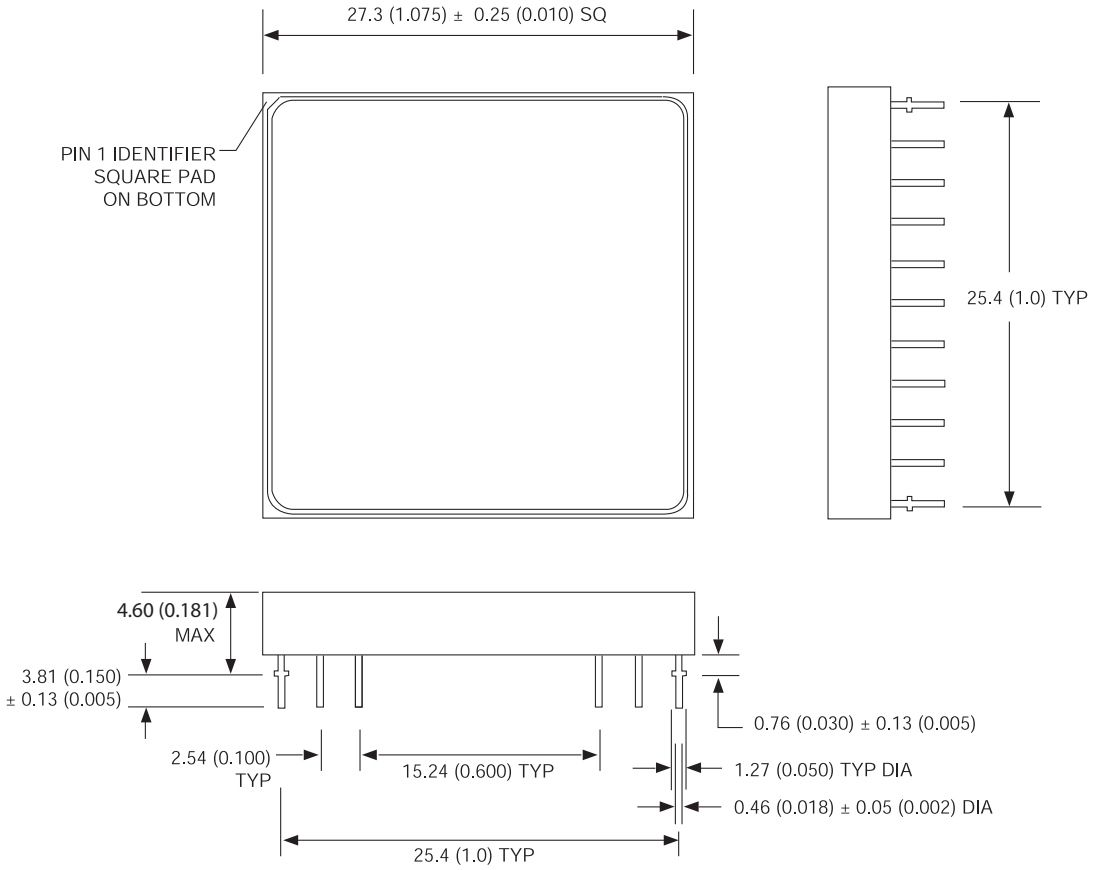
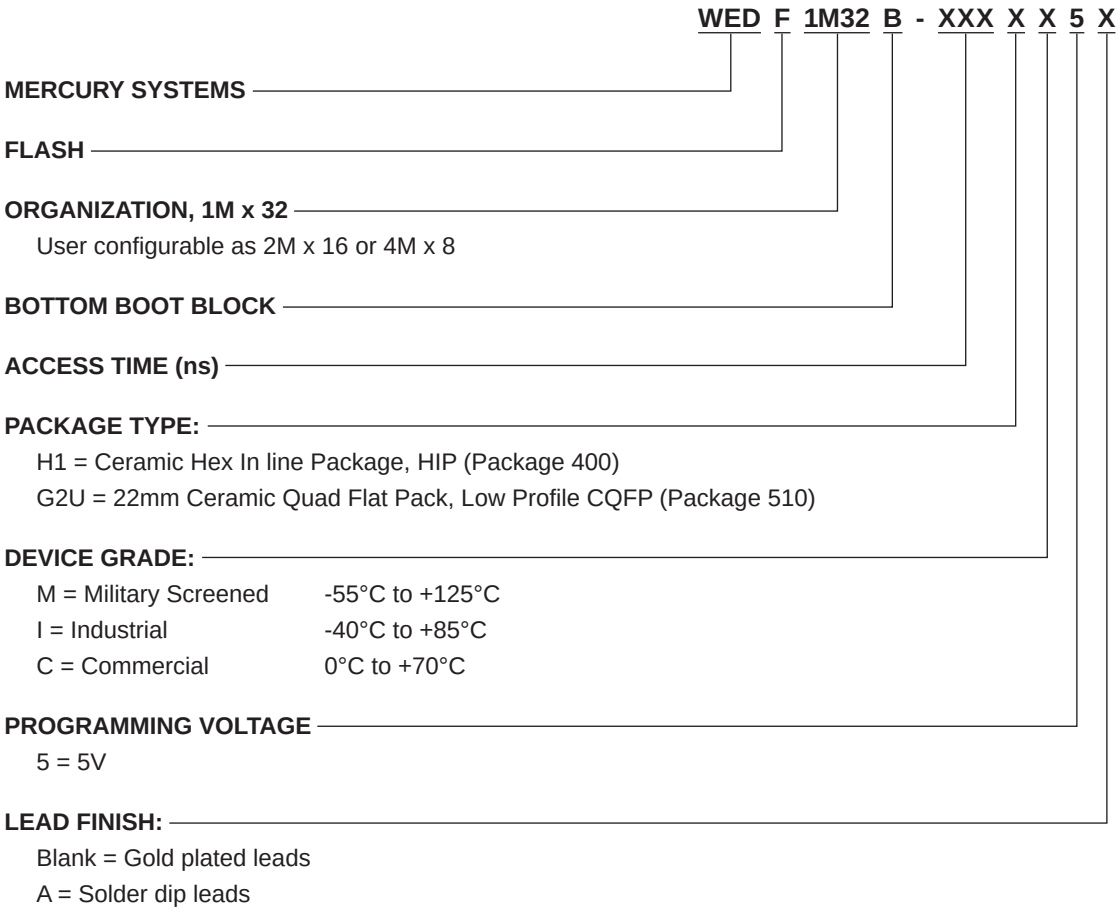
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 400 – 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



Document Title

1Mx32 5V NOR FLASH MODULE

Revision History

Rev #	History	Release Date	Status
Rev 3	Changes (Pg. 1-9) 3.1 Change document layout from White Electronic Designs to Microsemi 3.2 Add document Revision History page	June 2011	Advanced
Rev 4	Changes (Pg. 1, 9) 4.1 Add "NOR" to headline	August 2011	Advanced
Rev 5	Changes (Pg. 6) (ECN 9936) 5.1 Data sheet status changed from Advanced to Final 5.2 Update package dimensions	April 2016	Final
Rev 6	Changes (Pg. All) (ECN 10156) 6.1 Change document layout from Microsemi to Mercury Systems	August 2016	Final