

2Mx8 MONOLITHIC NOR FLASH SMD 5962-97609*



WMF2M8-XXX5

FEATURES

- Access Times of 90, 120, 150ns
- Packaging:
 - 56 lead, Hermetic Ceramic, 0.520" CSOP (Package 207). Fits standard 56 SSOP footprint.
 - 44 pin Ceramic LCC**
- Sector Architecture
 - 32 equal size sectors of 64KBytes each
 - Any combination of sectors can be erased. Also supports full chip erase.
- 100,000 Write/Erase Cycles Minimum
- Organized as 2Mx8
- Commercial, Industrial, and Military Temperature Ranges
- 5V Read and Write
- Low Power CMOS

- Data# Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- RESET# pin resets internal state machine to the read mode.
- Multiple Ground Pins for Low Noise Operation

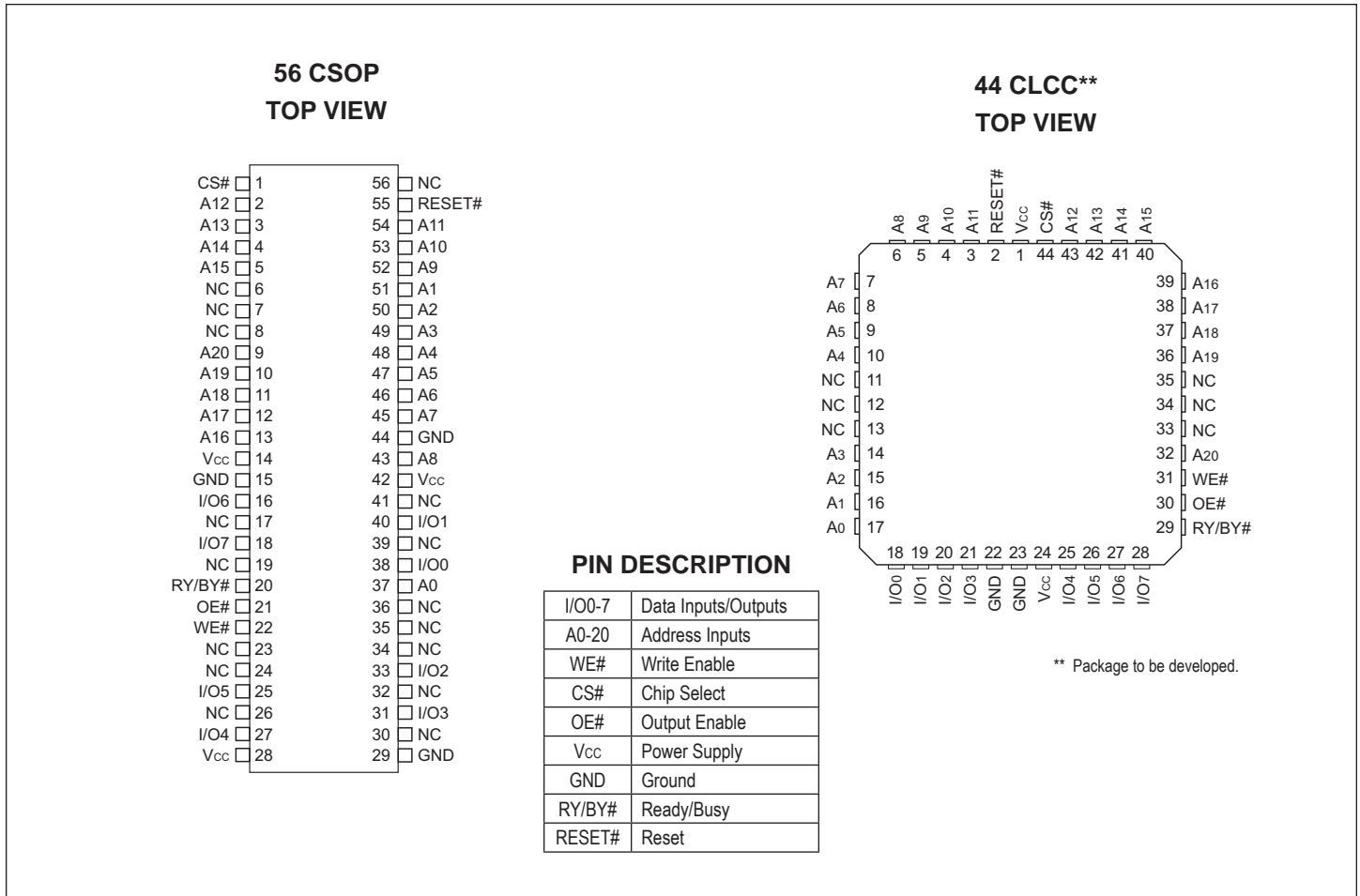
This product is subject to change without notice.

* For reference only. See table page 7.

** Package to be developed.

Note: For programming information and waveforms refer to Flash Programming 16M5 Application Note AN0038.

FIGURE 1 – PIN CONFIGURATION FOR WMF2M8-XXX5



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	-2.0 to +7.0	V
Storage Temperature	T _{STG}	-65 to +150	°C
Endurance - Write/Erase Cycles (Mil Temp)		100,000 min	cycles
Data Retention (Mil Temp)		20	years

NOTES:

- Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. See . Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See .
- Minimum DC input voltage on A9, OE#, RESET# pins is -0.5V. During voltage transitions, A9, OE#, RESET# pins may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. See Maximum DC input voltage on A9, OE#, and RESET# is 12.5 V which may overshoot to 13.5 V for periods up to 20 ns.

Stresses greater than those listed in this section may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	-	+0.8	V
Operating Temperature (Mil.)	T _A	-55	-	+125	°C
Operating Temperature (Ind.)	T _A	-40	-	+85	°C
Operating Temperature (Com.)	T _A	0	-	+70	°C

DC CHARACTERISTICS — CMOS COMPATIBLE

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = V _{CC MAX} , V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	V _{CC} = V _{CC MAX} , V _{OUT} = GND to V _{CC}		10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz		40	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	CS# = V _{IL} , OE# = V _{IH}		60	mA
V _{CC} Standby Current	I _{CC3}	V _{CC} = V _{CC MAX} , CS# = V _{CC} ± 0.5V, f = 5MHz, RESET# = V _{CC} ± 0.5V		2.0	mA
Output Low Voltage	V _{OL}	I _{OL} = 12.0 mA, V _{CC} = V _{CC MIN}		0.45	V
Output High Voltage	V _{OH}	I _{OH} = -2.5 mA, V _{CC} = V _{CC MIN}	0.85xV _{CC}		V
Low V _{CC} Lock-Out Voltage	V _{LKO}		3.2	4.2	V

NOTES:

- The I_{CC} is typically less than 2mA/MHz, with OE# at V_{IH}.
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.

CAPACITANCET_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
Address Input capacitance	C _{AD}	V _{I/O} = 0 V, f = 1.0MHz	12	pF
Output Enable capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0MHz	12	pF
Write Enable capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0MHz	12	pF
Chip Select capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0MHz	12	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0MHz	12	pF

This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – WE# CONTROLLED

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	90		120		150		ns
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	45		50		50		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	45		50		50		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
Address Hold Time	t _{WLAX}	t _{AH}	45		50		50		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t _{WHWH1}			300		300		300	μs
Sector Erase (2)	t _{WHWH2}			15		15		15	sec
Read Recovery Time before Write	t _{GHWL}		0		0		0		μs
V _{CC} Setup Time	t _{VCS}		50		50		50		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t _{OEHL}	10		10		10		ns
RESET# Pulse Width		t _{RP}	500		500		500		ns

NOTES:

1. Typical value for t_{WHWH1} is 7μs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	90		120		150		ns
Address Access Time	t _{AVQV}	t _{ACC}		90		120		150	ns
Chip Select Access Time	t _{ELQV}	t _{CE}		90		120		150	ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		40		50		55	ns
Output Enable Hold Time	Read Toggle &	t _{OEHL}	0		0		0		ns
	Data Polling		10		10		10		ns
Chip Select High to Output High Z (1)	t _{EHQZ}	t _{DF}		20		30		35	ns
Output Enable High to Output High Z (1)	t _{GHQZ}	t _{DF}		20		30		35	ns
Output Hold from Addresses, CS# or OE# Change, whichever is First	t _{AXQX}	t _{OH}	0		0		0		ns
RESET# Low to Read Mode (1)		t _{Ready}		20		20		20	μs

1. Guaranteed by design, not tested.

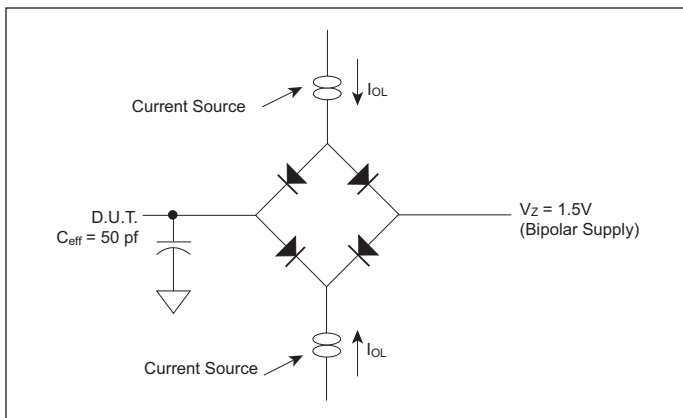
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, CS# CONTROLLED

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	μ s
Sector Erase Time (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time	t_{GHEL}		0		0		0		μ s
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEHL}	10		10		10		ns

NOTES:

1. Typical value for t_{WHWH1} is 7 μ s.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

FIGURE 2 – AC TEST CIRCUIT



AC Test Conditions

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

- V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance $Z_0 = 75 \Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.

HARDWARE RESET (RESET#)

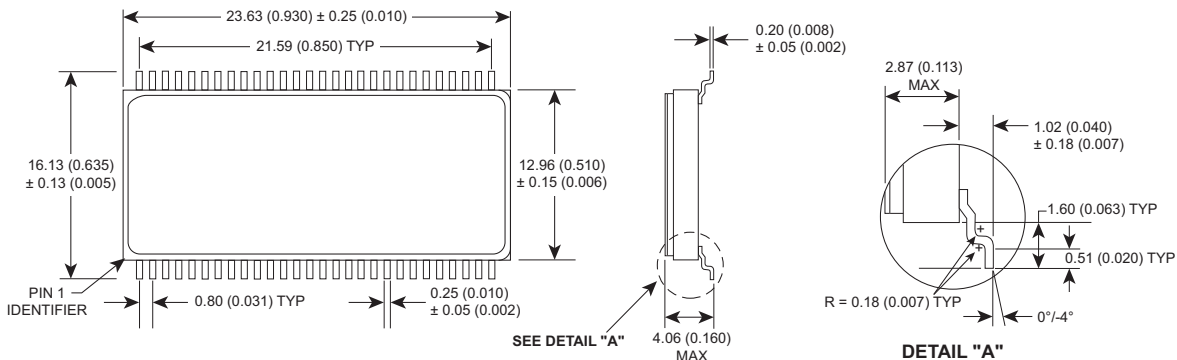
Parameter				
Std	Description	Test Setup	All Speed Options	Unit
t_{READY}	RESET Pin Low (During Embedded Algorithms) to Read or Write (See Note)	Max	20	μ s
t_{READY}	RESET Pin Low (Not During Embedded Algorithms) to Read or Write (See Note)	Max	500	ns
t_{RP}	RESET Pulse Width	Min	500	ns
t_{RH}	RESET High Time Before Read (See Note)	Min	50	ns
t_{RB}	RY/BY Recovery Time	Min	0	ns

TEMPORARY SECTOR UNPROTECTED

Parameter				
Std	Description		All Speed Options	Unit
tVIDR	VID Rise and Fall time (see notes)	Min	500	ns
tRSP	RESET# setup time for temporary sector unprotect	Min	4	ms

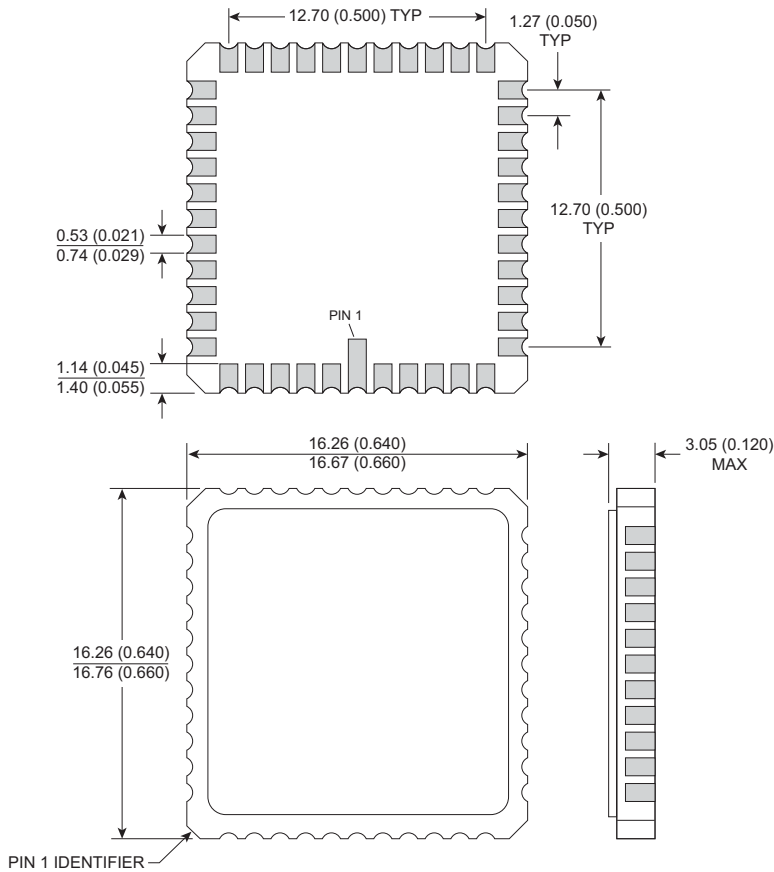
NOTE:
Not 100% tested.

PACKAGE 207 – 56 LEAD, CERAMIC SOP



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE DIMENSION – 44 LEAD, CERAMIC LCC**



** Package to be developed.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

	W M F 2M 8 - XXX X X 5 X
MERCURY SYSTEMS _____	
MONOLITHIC _____	
NOR FLASH _____	
ORGANIZATION, 2M x 8 _____	
ACCESS TIME (ns) _____	
PACKAGE TYPE: _____	
DA = 56 Lead CSOP (Package 207) fits standard 56 SSOP footprint	
L = 44 Lead Ceramic LCC*	
DEVICE GRADE: _____	
M = Military, 883 Screened -55°C to +125°C	
I = Industrial -40°C to +85°C	
C = Commercial 0°C to +70°C	
V _{PP} PROGRAMMING VOLTAGE _____	
5 = 5V	
LEAD FINISH: _____	
Blank = Gold plated leads	
A = Solder dip leads	

* Package to be developed.

DEVICE TYPE	SECTOR SIZE	SPEED	PACKAGE	SMD NO.
2M x 8 Flash Monolithic	64KByte	150ns	56 lead CSOP (DA)	5962-97609 01HXX
2M x 8 Flash Monolithic	64KByte	120ns	56 lead CSOP (DA)	5962-97609 02HXX
2M x 8 Flash Monolithic	64KByte	90ns	56 lead CSOP (DA)	5962-97609 03HXX

NOTE: This table is for reference only. For 5962-97609 ordering information and specifications refer to latest SMD document.

Document Title

2Mx8 MONOLITHIC NOR FLASH, SMD 5962-97609

Revision History

Rev #	History	Release Date	Status
Rev 7	Changes (Pg. 1-15) 7.1 Change document layout from White Electronic Designs to Microsemi 7.2 Add document Revision History page	June 2011	Final
Rev 8	Changes (Pg. 1, 15) 8.1 Add "NOR" to headline	August 2011	Final
Rev 9	Changes (Pg. 1-14) 9.1 Update features 9.2 Update <i>Absolute Maximum Ratings, Recommended DC Operating Conditions</i> and <i>DC Characteristics</i> charts 9.3 Delete subtitles from the <i>AC Characteristics</i> charts 9.4 Delete waveforms diagrams 9.5 Update package 207 and 44 Lead Ceramic LCC diagrams 9.6 Update ordering information and SMD charts	June 2012	Final
Rev 10	Change (Pg. 6) (ECN 9789) 10.1 Changed lead dimensions on Package 207	January 2016	Final
Rev 11	Changes (Pg. All) (ECN 10156) 11.1 Change document layout from Microsemi to Mercury Systems	August 2016	Final