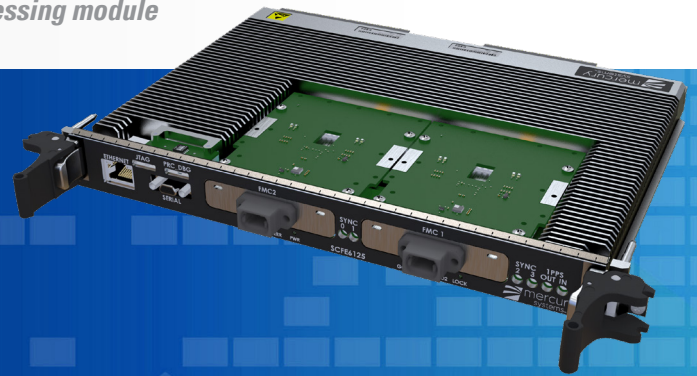## mercury systems

EnsembleSeries™ SCFE6125

Configurable, low-latency, OpenVPX™ Optical Fiber FPGA processing module

- **Virtex UltraScale+ FPGA Processing Power**

- **Processing subsystem in data path for max performance**

- **OpenVPX™ compliant for easy integration**

- **Multiple high-reliability cooling options**

Mercury's EnsembleSeries™ SCFE6125 is a versatile OpenVPX FPGA processing module designed for high performance with integrated optical fiber FMCs. Incorporating Zynq Ultrascale+™ FPGA processing power and an open architecture, this advanced module maximizes performance by locating the processing sub-system directly in the data path. With multiple cooling options available, the SCFE6125 is ideal for applications that require high-performance operation in harsh environments.

High Data Rate Optical Interface

Currently implemented at 10.3125Gbps, the SCFE6125 has integrated Fiber FMC boards for connectivity to external system components. Each VU9P FPGA has a FMC connected that provides the required 8Rx/8Tx fiber links per FPGA. The fiber connection is implemented with a MPO-24 fiber male connector.

Mercury's processing modules are built around our EchoCore® FPGA IP to provide basic infrastructure functionality right out of the box. Mercury facilitates the re-use of common IP across FPGAs to optimize time-to-market and reduce development time. EchoCore IP allows customers to focus on their application while building upon the groundwork provided.

Mercury simplifies application integration by providing a standard control plane interface using AXI4-Lite control

plane connectivity. Mercury uses a simple AXI4-Stream interface for our data plane with AXI4-Stream switches for routing data within the FPGA and to external interfaces, such as PCIe. Our customers can choose their tool of choice, such as parameterizable Xilinx IPs, HLS, or RTL to generate signal processing algorithms. The cores are then instantiated into a reserved user block and compiled into the FPGAs.

Specifications

Physical
Single Slot 6U OpenVPX form factor
OpenVPX interface compliant with FMC ANSI/VITA 57.4

Optical Sites
Each Fiber FMC: 12 Rx links (1-8 used) and 12 Tx links (1-8 used)

Backplane Interface
VITA 65.0 slot profile SLT6-PAY-4F1Q1H2U2T1H-10.6.1-n.

FPGA processors
Two Xilinx Virtex® Ultrascale+™ VU9P Prosecutors
One Xilinx Zynq® Ultrascale+™ ZU11EG Governor

Memory
20 GB of DDR4 SDRAM

Other
Vita 46.11 IPMI controller
Sensor interface to monitor temperature, voltage
Power sequencing
Secure JTAG
Manufactured in an AS9100D facility
Advanced FPGA Functionality

Mercury Systems is a leading commercial provider of secure sensor and safety-critical processing subsystems. Optimized for customer and mission success, Mercury's solutions power a wide variety of critical defense and intelligence programs.
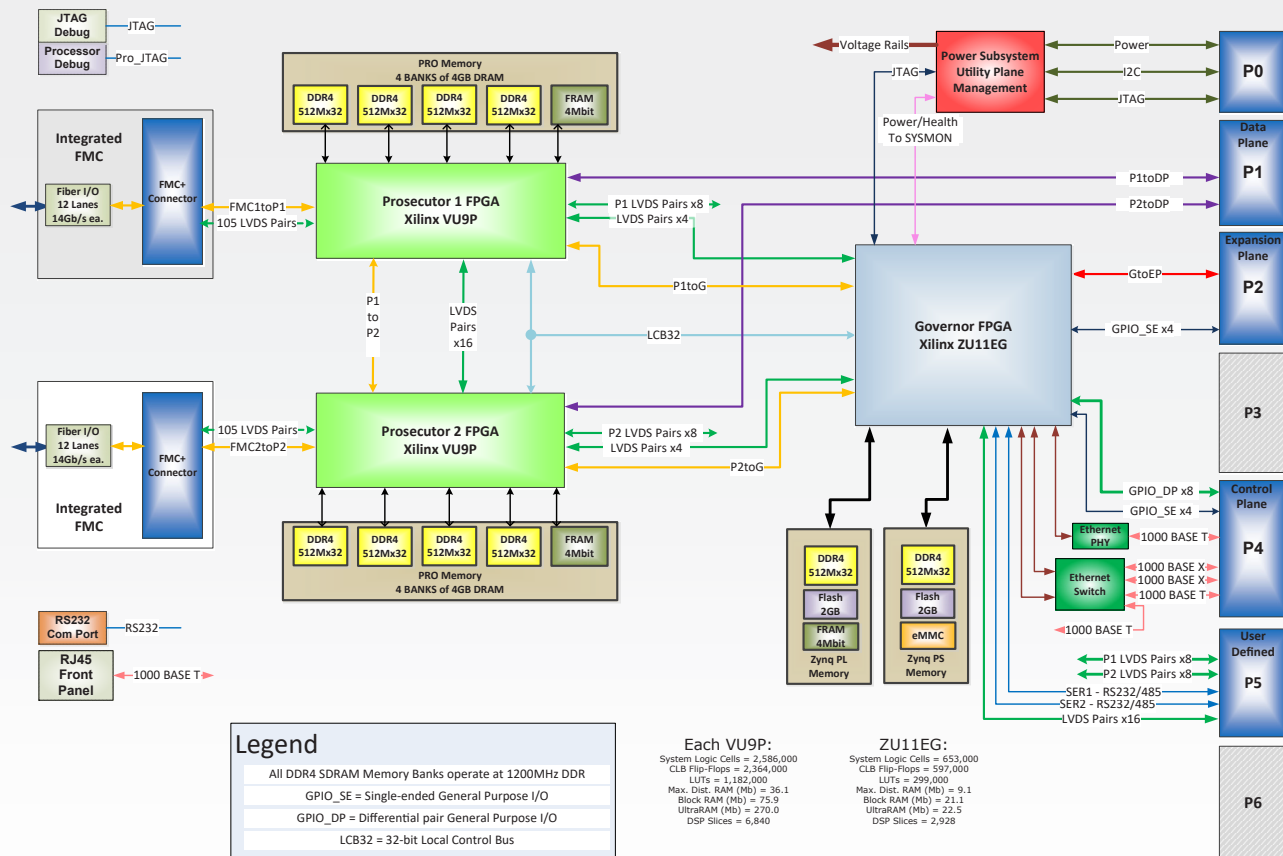
ACQUIRE   DIGITIZE   PROCESS   STORAGE S   EXPLOIT   DISSEMINATE

JTAG Debug —JTAG—
Processor Debug —Pro_JTAG—

PRO Memory
4 BANKS of 4GB DRAM
DDR4 512Mx32 | DDR4 512Mx32 | DDR4 512Mx32 | DDR4 512Mx32 | FRAM 4Mbit

Integrated FMC
Fiber I/O 12 Lanes 14Gb/s ea. — FMC+ Connector
—FMC1toP1—
—105 LVDS Pairs—

Prosecutor 1 FPGA Xilinx VU9P
—P1 LVDS Pairs x8—
—LVDS Pairs x4—

P1 to P2

LVDS Pairs x16

LCB32

Prosecutor 2 FPGA Xilinx VU9P
—105 LVDS Pairs—
—FMC2toP2—
—P2 LVDS Pairs x8—
—LVDS Pairs x4—
—P2toG—

Integrated FMC
Fiber I/O 12 Lanes 14Gb/s ea. — FMC+ Connector

DDR4 512Mx32 | DDR4 512Mx32 | DDR4 512Mx32 | DDR4 512Mx32 | FRAM 4Mbit
PRO Memory
4 BANKS of 4GB DRAM

RS232 Com Port —RS232—
RJ45 Front Panel —1000 BASE T—

—P1toG—

Voltage Rails —
Power Subsystem Utility Plane Management
—JTAG—
Power/Health To SYSMON

—Power—
—I2C—
—JTAG—
P0

Data Plane P1
—P1toDP—
—P2toDP—

Expansion Plane P2
—GtoEP—
—GPIO_SE x4—

Governor FPGA Xilinx ZU11EG

P3

DDR4 512Mx32 | Flash 2GB | FRAM 4Mbit
Zynq PL Memory

DDR4 512Mx32 | Flash 2GB | eMMC
Zynq PS Memory

Ethernet PHY —1000 BASE T—
Ethernet Switch —1000 BASE X— —1000 BASE X— —1000 BASE T—
—1000 BASE T—

—GPIO_DP x8—
—GPIO_SE x4—

Control Plane P4

User Defined P5
—P1 LVDS Pairs x8—
—P2 LVDS Pairs x8—
—SER1 - RS232/485—
—SER2 - RS232/485—
—LVDS Pairs x16—

P6

Legend

All DDR4 SDRAM Memory Banks operate at 1200MHz DDR
GPIO_SE = Single-ended General Purpose I/O
GPIO_DP = Differential pair General Purpose I/O
LCB32 = 32-bit Local Control Bus

Each VU9P:
System Logic Cells = 2,586,000
CLB Flip-Flops = 2,364,000
LUTs = 1,182,000
Max. Dist. RAM (Mb) = 36.1
Block RAM (Mb) = 75.9
UltraRAM (Mb) = 270.0
DSP Slices = 6,840

ZU11EG:
System Logic Cells = 653,000
CLB Flip-Flops = 597,000
LUTs = 299,000
Max. Dist. RAM (Mb) = 9.1
Block RAM (Mb) = 21.1
UltraRAM (Mb) = 22.5
DSP Slices = 2,928

SCFE6125 functional block diagram

Application Notes

Multiple generations of this product family protect have provided the signal processing functionality that enables systems to nimbly respond to emerging threats. Examples include:

- Wideband search using full sample-rate FFTs and threshold detection processing
- Channelizers and multiple independent/coherent digital down/ up converter channels with integrated filtering, gain balancing, high precision receive time tagging and transmit scheduling, VITA 49.2 signal data and context packet generation and reception / depacketizing
- Non-coherent and low latency coherent EA technique generation
- Communications modem functions

Instantaneous Bandwidths (IBW) in excess of 1 GHz have been implemented and transferred, as well as multiple simultaneous down-converted signal streams of over 100 MHz IBW.

Need more help? Need a variant of this product?

Contact Mercury's Mixed Signal Engineering team at: digital.rf@mrcy.com or
visit www.mrcy.com/mixed-signal-processing for a detailed listing of OpenVPX products.

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