The Ensemble® HDS6601 is a high-density server signal and data processing engine, harnessing two of the latest generation of server-class Sandy Bridge octal-core Intel® Xeon® processors for the most demanding applications. The HDS6601 combines this processing performance with a next-generation Protocol Offload Engine Technology (POET™) fabric bridge, scaling the module’s I/O infrastructure to match the unparalleled embedded processing performance of server-class Intel processors.

By leveraging the power of Intel server-class processing in combination with the on-board integrated high-performance PCIe® and fabric infrastructure, the HDS6601 delivers a well-balanced and scalable computing architecture. The HDS6601 is capable of providing ground-breaking levels of processing power for high-end radar, signal intelligence and image processing applications, as well as data-intensive commercial applications, in a standard 6U OpenVPX™ form factor.

**Intel Xeon Sandy Bridge Server-Class Processor**

The HDS6601 features two 64-bit Xeon E5-2648LE Sandy Bridge-class octal core processors. Following on technology first deployed on the HDS6600, the HDS6601 utilizes unique packaging technologies to support two instances of 2011-pin Land Grid Array (LGA) processors in a rugged, embedded form factor. The dual octal-core processors are linked via two instances of the high-speed, low-latency QPI interface, each of which provides a 25.6 GB/s transfer rate, for a staggering total of 51.2 GB/s of bandwidth between processors.

This interconnected processor architecture is optimized for the intense data movement needed by processing algorithms, such as all-to-all corner turn operations. From a software perspective, this QPI architecture allows the HDS6601 to be configured with a single kernel NUMA-aware operating system running across both processor devices. Each processor is capable of delivering approximately 230 GFLOPS (peak), with four high-speed DDR3-1600 memory channels capable of 12.8 GB/s raw bandwidth each, for an incredible total peak of 460 GFLOPS and 102.4 GB/s total raw memory bandwidth.

The HDS6601 refines the innovative standing memory technology first seen on the HDS6600 to support 32 GB of DRAM on-board for the ultimate in DRAM density in the OpenVPX family of processing modules. Native PCIe support is also featured on this processor, linking the processing resources directly to the I/O sources on the module. The HDS6601 also makes use of the Patsburg-B Platform Controller Hub (PCH) chipset, which provides additional I/O bridging between the Intel processor and external devices.

Mercury Systems is a best-of-breed provider of commercially developed, open sensor and Big Data processing systems, software and services for critical commercial, defense and intelligence applications.
The E5-2648L processor includes a very large 20MB cache, shared between the cores, allowing many high-performance calculations to remain cache resident. This accelerates processing by eliminating the potential latency required to access DRAM to fetch upcoming data. The Sandy Bridge family of processors also supports the newly introduced AVX instruction set, delivering a revolutionary increase in floating-point high-performance algorithm performance that is portable to future Intel architectures.

High-Speed Fabric Interfaces

The HDS6601 continues the Mercury Systems tradition of combining the processing power of Intel processors with a high-speed Serial RapidIO® or 10 Gigabit Ethernet fabric interface. The on-board Virtex® 6 FPGA can be configured with IP that provides a streaming bridge for high-bandwidth, low-latency data. The HDS6601 supports either Serial RapidIO (Gen2) or 10 Gigabit Ethernet bridging to the native PCIe interface on the Intel processor. The HDS6601 improves on previous generations in the HDS family by providing a full complement of four x4 data plane interfaces to the backplane. By linking the Intel processor with a high-performance OpenVPX™ data plane, the HDS6601 architecture ensures an optimal balance between I/O and processing capabilities.

PCI Express Architecture

The HDS6601 provides high-end PCIe backplane interfaces via the native PCIe resources on the E5-2648L processor. In addition to supporting the processor’s interface to the POET bridge described earlier, an additional x16 PCIe interface is provided to the OpenVPX expansion plane interface on both the P2 and P5 VPX connectors. These interfaces enable the HDS6601’s compatibility with Mercury’s GPU, FPGA or mezzanine carrier modules. The interfaces are user configurable to lower port widths. These configuration options support the construction of complex PCIe trees with many other PCIe-capable devices.

Multiple I/O Options

The HDS6601 offers a variety of additional built-in I/O options:

- One 10/100/1000BASE-T Gigabit Ethernet connection routed to the front panel on air-cooled configurations or to the backplane on conduction-cooled configurations.
- One additional 10/100/1000BASE-T Gigabit Ethernet connection routed to the backplane.
- Two 1000BASE-BX SERDES Ethernet connections routed to the backplane as per the OpenVPX control plane specification.
- One RS-232 serial port is routed to the front panel on air-cooled configurations, or to the backplane on conduction-cooled configurations. When routed to the backplane, the serial interface can be configured for either RS-232 or RS-422 signaling.
- One additional RS-422 interface and two RS-232 interfaces are routed to the backplane.
- One front panel USB2.0 interface on air cooled configurations only.
- Two backplane USB2.0 interfaces, available with both air-cooled and conduction-cooled configurations.
- One front panel eSATA interface on air-cooled configurations only.
- Two SATA interfaces to the backplane are provided to easily interface with storage devices.
- Eight GPIO lines act as discrete I/O, usable as input, output or to generate interrupts on the module.
- Several additional bussed signals that enhance the functionality of the HDS6601 module.

System Management

The HDS6601 module implements the advanced system management functionality architected in the OpenVPX Specification to enable remote monitoring, alarm management and hardware revision and health status.

Using the standard I2C bus and Intelligent Platform Management Interface (IPMI) protocol, the on-board system management block implements the Intelligent Platform Management Controller (IPMC), in accordance with the VITA 46.11 standard. This allows the HDS6601 module to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage or current variations that exceed those thresholds
- Reset the entire module
- Power up/down the entire module
- Retrieve module Field Replaceable Unit (FRU) information
- Be managed remotely by a Chassis Management Controller at the system level, such as implemented on the OpenVPX™ SFM6101 and SFM6102 series of Switch Fabric Modules

VPX-REDI

The VPX™ (VITA 46) standard defines 6U and 3U board formats with a modern high-performance connector set capable of supporting today’s high-speed fabric interfaces. VPX is most attractive when paired with the Ruggedized Enhanced Design Implementation standard — REDI (VITA 48). The HDS6601 module is implemented as a 6U conduction-cooled implementation of VPX-REDI, with air-cooled variants in the same VPX form factor available for less rugged environments. Targeted primarily for harsh-environment embedded applications, VPX-REDI offers extended mechanical configurations supporting higher functional density, such as Two-Level Maintenance (2LM). 2LM allows relatively unskilled maintenance personnel to replace a failed module and restore the system to an operational state in a limited time period, minimizing potential damage to the module.
Additional Features

The HDS6601 provides all the features typically found on a single-board computer. In addition to the sophisticated management subsystem and fabric interconnect, it provides users with a toolkit enabling many different application use cases.

Features include:

- Thermal and voltage sensors integrated on-board
- Real-time clock with granularity to 1 ms and time measurement of up to 30 years
- General-purpose timers
- Global clock synchronization capabilities via the OpenVPX utility plane clock signals
- Watchdog timer to support interrupt or reset
- Multiple boot paths, including netboot, USB boot, and boot from SATA or the on-board 8 GB flash device

Open Software Environment

Mercury leverages over 25 years of multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the HDS6601 module. Because the processor, memory and surrounding technologies are leveraged across product lines, software developed on the HDS6601 module can interface seamlessly with other Mercury products. The same development and run-time environment is implemented on the HDS6601 module as on other Mercury platforms across the Ensemble 3000, 5000 and 6000 series.

The MultiCore Plus (MCP) open software environment gives the HDS6601 module access to a wide ecosystem of stacks, middleware, libraries and tools. Software support is available on the HDS6601 module for the following products:

Support for Mercury’s standard numeric libraries via the MathPak product, which includes Vector Signal Image Processing Library (VSIPL) and Scientific Algorithm Library (SAL), is optimized for the Intel AVX architecture of the HDS6601 module.

Open Development Suite for Linux® is an Eclipse-based integrated development environment that includes a C/C++ optimizing compiler, a source-level debugger, a language-sensitive text editor, a performance profiler, a project builder, a version control system, a run-time error checker and a graphical source browser. Mercury provides extensions that allow multiprocessor-aware process launch and debug, as well as a System Supervisor view that allows graphical remote management.

Support is provided for Wind River® Workbench integrated development environment when the module is running Wind River Linux® or VxWorks®.
Interprocessor Communication System (ICS) support is carried forward from the RACE++/MCOE software environment. ICS provides a low-level interprocessor communication API that lets users take advantage of the high-bandwidth, low-latency Serial RapidIO fabric with an easy-to-use software interface. OpenMPI/OFED middleware support pairs an open, recognized software interface with Mercury's optimization at the fabric level for unparalleled performance for data transfers over the data plane fabric.

- Trace Analysis Tool and Library (TATL™) is a 'logic analyzer for software’ that provides insight into the dynamic interaction of up to a few hundred processors.

The MCP software environment lets applications use industry-standard middleware such as MPI, DRI, CORBA or standard TCP/IP sockets ported to run seamlessly over the fabric. MCP also offers a software tool that can help migrate legacy applications created with MCOE™ into the MCP domain.

**Open Standards Mean Interoperability and Planning for the Future**

The OpenVPX Industry Working Group was an industry initiative launched by defense prime contractors and Commercial-Off-The-Shelf (COTS) system developers to take a proactive approach to solving the interoperability issues associated with the VITA 46 (VPX) family of specifications. This group has created an overarching System Specification defining VPX system architecture through pinout definitions to establish a limited set of application-specific reference solutions. These OpenVPX standard solutions provide clear design guidance to COTS suppliers and the user community, assuring interoperability across multi-vendor implementations. The OpenVPX System Specifications were ratified by the VSO in February 2010.

**Specifications**

**Intel 32-nm Sandy Bridge–Class Processor**

Two Octal-core E5-2648L Sandy Bridge server-class processors at 1.8 GHz each
- Peak performance 460 GFLOPS
- Threads per core 2
- QPI interface between processors 2 x 25.6 GB/s peak performance
- Intel Virtualization Technology
- Dual Integrated x16 Gen2 PCIe interface
- DOR3-1600 32 GB with ECC
- Raw memory bandwidth 102 GB/s
- BIOS SPI flash Dual 8 MB partitions
- NAND flash 8 GB, SATA interface

**Virtex® 6 HX380T Field-Programmable Gate Array (FPGA)**

Provides fabric bridging to data plane
Can act as co-processor executing iFFT/FFT, image or signal processing
Configured from CPU or dedicated configuration ROM

**Ethernet Connections**

1000BASE-BX Ethernet to P4 connector 2
- OpenVPX™ Control Plane
10/100/1000BASE-T Ethernet to P4 connector 1
- Accessible via OpenVPX RTM or external chassis interface
10/100/1000BASE-T Ethernet connection 1
- to front panel (air-cooled module), or
- to backplane (conduction-cooled module)

Ethernet functions supported by the chipset include:
- UDP, TCP, SCTP, ARP, IPv4, IPv6, IEEE 1588, flow control, 802.1P (priority), 802.1Q (VLAN)

**Intelligent Platform Management Interface (IPMI)**

On-board IPMI controller
- Voltage and temperature monitor
- Geographical address monitor
- Power/reset control
- FRU and on-board EEPROM interfaces
- FPGA, CPU and CPLD interfaces

**OpenVPX Multi-Plane Architecture**

System Management via IPMB-A and IPMB-B link on P0 management plane
- Dual 4x Serial RapidIO or 10 Gigabit Ethernet interfaces on P1 data plane
- Dual full x16 or dual x8 PCIe expansion plane
- Dual 1000BASE-BX Ethernet control plane

**Additional I/O Capabilities**

- RS-232 serial interface 1
  - to front panel (air-cooled), or
  - to backplane (conduction-cooled)
- Configurable for RS-422 signaling when routed to backplane
- RS-422 serial interface to backplane 1
- RS-232 serial interfaces to backplane 2
- Front-panel USB 2.0 interface 1
  - (air-cooled configurations only)
- USB 2.0 interfaces to backplane 2
- Front-panel eSATA interface 1
  - (air-cooled configurations only)
- SATA interfaces to backplane 2
- Single-ended GPIO interfaces to backplane 8
- System signals to backplane
- NVMR0, ChassisTest, Environmental Bypass, MemoryClear

**Mechanical**

- 6U OpenVPX (air-cooled and conduction-cooled)
- 1.0” slot pitch
- OpenVPX and VPX REDI
### Environmental Qualification Levels

<table>
<thead>
<tr>
<th>Environmental Qualification Levels</th>
<th>Commercial L0</th>
<th>Rugged L1</th>
<th>Rugged L2</th>
<th>Rugged L4</th>
<th>Rugged L3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Ruggedness</strong></td>
<td>*</td>
<td>**</td>
<td>**</td>
<td>***</td>
<td>***</td>
</tr>
<tr>
<td><strong>Moisture/dust protection</strong></td>
<td>*</td>
<td>**</td>
<td>**</td>
<td>***</td>
<td>***</td>
</tr>
<tr>
<td><strong>Typical cooling performance</strong></td>
<td>-140W**</td>
<td>-140W**</td>
<td>-150W**</td>
<td>-200W*</td>
<td>-150W**</td>
</tr>
<tr>
<td><strong>Temperature</strong></td>
<td>0ºC to +40ºC</td>
<td>-25ºC to +55ºC</td>
<td>-45ºC to +70ºC</td>
<td>-40ºC to +60ºC</td>
<td>-40ºC to +71ºC</td>
</tr>
<tr>
<td>Operating temperature maximum rate of change</td>
<td>N/A</td>
<td>10°C/min</td>
<td>10°C/min</td>
<td>10°C/min</td>
<td>10°C/min</td>
</tr>
<tr>
<td><strong>Temperature</strong></td>
<td>-40ºC to +85ºC</td>
<td>-55ºC to +85ºC</td>
<td>-55ºC to +125ºC</td>
<td>-55ºC to +125ºC</td>
<td>-55ºC to +125ºC</td>
</tr>
<tr>
<td><strong>Humidity</strong></td>
<td>10-90%, non-condensing</td>
<td>5-95%, non-condensing</td>
<td>5-95%, non-condensing</td>
<td>5-95%, non-condensing</td>
<td>5-95%, non-condensing</td>
</tr>
<tr>
<td>Storage</td>
<td>5-95%, non-condensing</td>
<td>5-95%, non-condensing</td>
<td>5-95%, non-condensing</td>
<td>5-95%, non-condensing</td>
<td>5-95%, non-condensing</td>
</tr>
<tr>
<td><strong>Altitude</strong></td>
<td>0-10,000ft</td>
<td>0-30,000ft</td>
<td>0-30,000ft</td>
<td>0-30,000ft</td>
<td>0-70,000ft</td>
</tr>
<tr>
<td>Storage</td>
<td>0-30,000ft</td>
<td>0-50,000ft</td>
<td>0-50,000ft</td>
<td>0-50,000ft</td>
<td>0-70,000ft</td>
</tr>
<tr>
<td><strong>Random</strong></td>
<td>0.003 g²/Hz; 20-2000 Hz, 1 hr/axis</td>
<td>0.04 g²/Hz; 20-2000 Hz, 1 hr/axis</td>
<td>0.04 g²/Hz; 20-2000 Hz, 1 hr/axis</td>
<td>0.1 g²/Hz; 5-2000 Hz, 1 hr/axis</td>
<td>0.1 g²/Hz; 5-2000 Hz, 1 hr/axis</td>
</tr>
<tr>
<td><strong>Sine</strong></td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>10G peak; 5-2000 Hz, 1 hr/axis</td>
<td>10G peak; 5-2000 Hz, 1 hr/axis</td>
</tr>
<tr>
<td><strong>Shock</strong></td>
<td>20g; (11ms 1/2-sine pulse, 3 positive, 3 negative)</td>
<td>50g; (11ms 1/2-sine pulse, 3 positive, 3 negative)</td>
<td>50g; (11ms 1/2-sine pulse, 3 positive, 3 negative)</td>
<td>50g; (11ms 1/2-sine pulse, 3 positive, 3 negative)</td>
<td>50g; (11ms 1/2-sine pulse, 3 positive, 3 negative)</td>
</tr>
<tr>
<td><strong>VITA 47</strong></td>
<td>N/A</td>
<td>Contact Factory</td>
<td>Contact Factory</td>
<td>10% NaCl</td>
<td>10% NaCl</td>
</tr>
</tbody>
</table>

* Customer must maintain required cfm level. Consult factory for the required flow rates.
** Card edge should be maintained below 71ºC.

Storage Temperature is defined per MIL-STD-810F, Method 502.4, para 4.5.2, where the product under non-operational test is brought to an initial high temperature cycle to remove moisture. Then the unit under non-operational test will be brought to the low storage temperature. The low temperature test is maintained for 2 hours. The product is then brought back to ambient temperature. All temperature transitions are at a maximum rate of 10ºC/min. One cold/hot cycle constitutes the complete non-operational storage temperature test. This assumes that the board level products are individually packaged in accordance with ASTM-D-3951 approved storage containers. These tests are not performed in Mercury shipping containers, but in an unrestrained condition. Please consult the factory if you would like additional test details.

All products manufactured by Mercury meet elements of the following specifications: MIL-STD-454, MIL-STD-883, MIL-HDBK-217F, and MIL-I-46058 or IPC-CC-830, and various IPC standards. Mercury’s inspection system has been certified in accordance with MIL-I-45208A.

### Additional Services

<table>
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<tr>
<th>Optional Environmental Screening and Analysis Services</th>
<th>Standard Module, Optional Services</th>
</tr>
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<tr>
<td>• Cold Start Testing</td>
<td>• Engineering Change Order (ECO) Notification</td>
</tr>
<tr>
<td>• Cold Soak Testing</td>
<td>• Alternate Mean Time Between Failure (MTBF) Calculations</td>
</tr>
<tr>
<td>• Custom Vibration</td>
<td>• Hazmat Analysis</td>
</tr>
<tr>
<td>• CFD Thermal Analysis</td>
<td>• Diminished Manufacturing Sources (DMS) Management</td>
</tr>
<tr>
<td>• Finite Element Analysis</td>
<td>• Longevity of Supply (LOS)</td>
</tr>
<tr>
<td>• Safety Margin Analysis</td>
<td>• Longevity of Repair (LOR)</td>
</tr>
<tr>
<td>• Temperature Cycling</td>
<td>Contact factory for additional information</td>
</tr>
<tr>
<td>• Power Cycling</td>
<td></td>
</tr>
<tr>
<td>• Environmental Stress Screening</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Safety Margin Analysis</th>
<th>ECO Control</th>
<th>Custom Certificate of Conformity (CoC)</th>
<th>Custom UID Labeling</th>
<th>Alternate Mean Time Between Failure (MTBF) Calculations</th>
<th>Hazmat Analysis</th>
<th>Diminished Manufacturing Sources (DMS) Management</th>
<th>Longevity of Supply (LOS)</th>
<th>Longevity of Repair (LOR)</th>
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